x2

EXTRA TOPICS RELATED TO

JFETs and GaAs Devices and Circuits

This supplement contains material removed from previous editions of the textbook. These topics continue to be relevant and for this reason will be of great value to many instructors and students.

The topics presented here relate to different kinds of FETs not discussed in the textbook. This material thus builds on material presented in Chapter 5 of the eighth edition.

x2.1 The Junction Field-Effect Transistor (JFET)

The **junction field-effect transistor,** or JFET, is perhaps the simplest transistor available. It has some important characteristics, notably a very high input resistance. Unfortunately, however (for the JFET), the MOSFET has an even higher input resistance. This, together with the many other advantages of MOS transistors, has made the JFET virtually obsolete. Currently, its applications are limited to discrete-circuit design, where it is used both as an amplifier and as a switch. Its integrated-circuit applications are limited to the design of the differential input stage of some operational amplifiers, where advantage is taken of its high input resistance (compared to the BJT). In this section, we briefly consider JFET operation and characteristics. Another important reason for including the JFET in the study of electronics is that it helps in understanding the operation of gallium arsenide devices, the subject of the next section.

x2.1.1 Device Structure

As with other FET types, the JFET is available in two polarities: *n*-channel and *p*-channel. Fig. x2.1(a) shows a simplified structure of the *n*-channel JFET. It consists of a slab of *n*-type silicon with *p*-type regions diffused on its two sides. The *n* region is the channel, and the *p*-type regions are electrically connected together and form the gate. The device operation is based on reverse-biasing the *pn* junction between gate and channel.

Indeed, it is the reverse bias on this junction that is used to control the channel width and hence the current flow from drain to source. The major role that the *pn* junction plays in the operation of this FET gives us its name: Junction Field-Effect Transistor (JFET).

It should be obvious that a *p*-channel device can be fabricated by simply reversing all the semiconductor types, thus using *p*-type silicon for the channel and *n*-type silicon for the gate regions.

Figures x2.1(b) and (c) show the circuit symbols for JFETs of both polarities. Observe that the device polarity (*n*-channel or *p*-channel) is indicated by the direction of the arrowhead on the gate line. This arrowhead points in the forward direction of the gate–channel *pn* junction. Although the JFET is a symmetrical device whose source and drain can be interchanged, it is useful in circuit design to designate one of these two terminals as source and the other as drain. The circuit symbol achieves this designation by placing the gate closer to the source than to the drain.

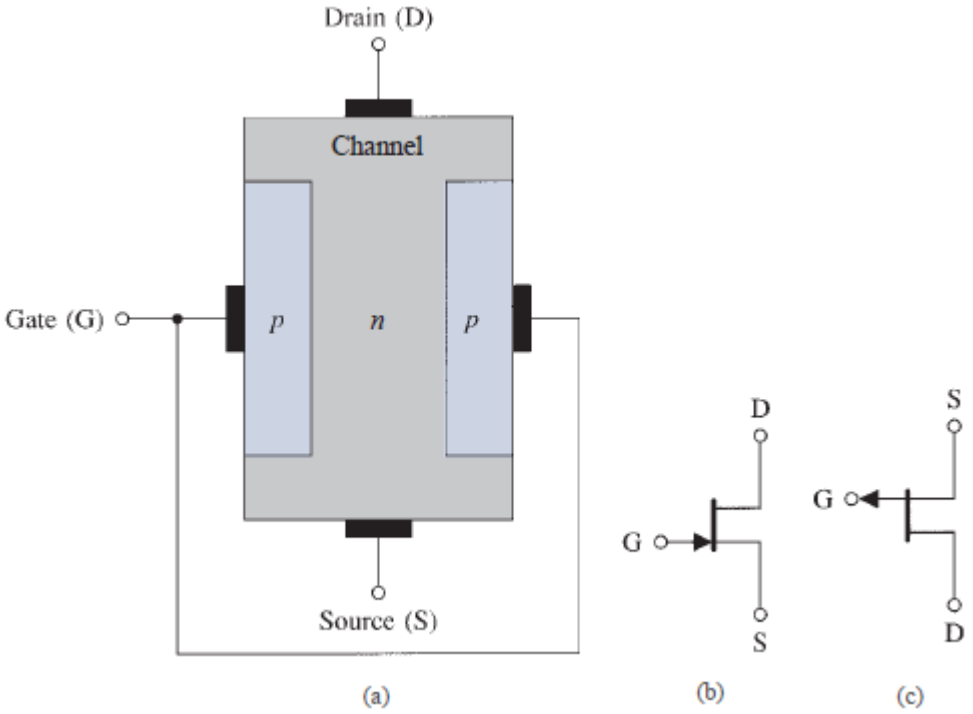


FIGURE x2.1 **(a)** Basic structure of *n*-channel JFET. This is a simplified structure utilized to explain device operation. **(b)** Circuit symbol for the *n*-channel JFET. **(c)** Circuit symbol for the *p*-channel JFET.

x2.1.2 Physical Operation

Consider an *n*-channel JFET and refer to Fig. x2.2(a). (Note that to simplify matters, we will not show the electrical connection between the gate terminals; it is assumed, however, that the two terminals labeled G are joined together.) With $v_{GS} = 0$, the application of a voltage v_{DS} causes current to flow from the drain to the source. When a negative v_{GS} is applied, the depletion region of the gate–channel junction widens and the channel becomes correspondingly narrower; thus the channel resistance increases and the current i_D (for a given v_{DS}) decreases. Because v_{DS} is small, the channel is almost of uniform width. The JFET is simply operating as a resistance whose value is controlled by v_{GS}. If we keep increasing v_{GS} in the negative direction, a value is reached at which the

depletion region occupies the entire channel. At this value of v_{GS} the channel is completely depleted of charge carriers (electrons); the channel has in effect disappeared. This value of v_{GS} is therefore the threshold voltage of the device, V_t, which is obviously negative for an *n*-channel JFET. For JFETs the threshold voltage is called the **pinch-off voltage** and is denoted V_P.

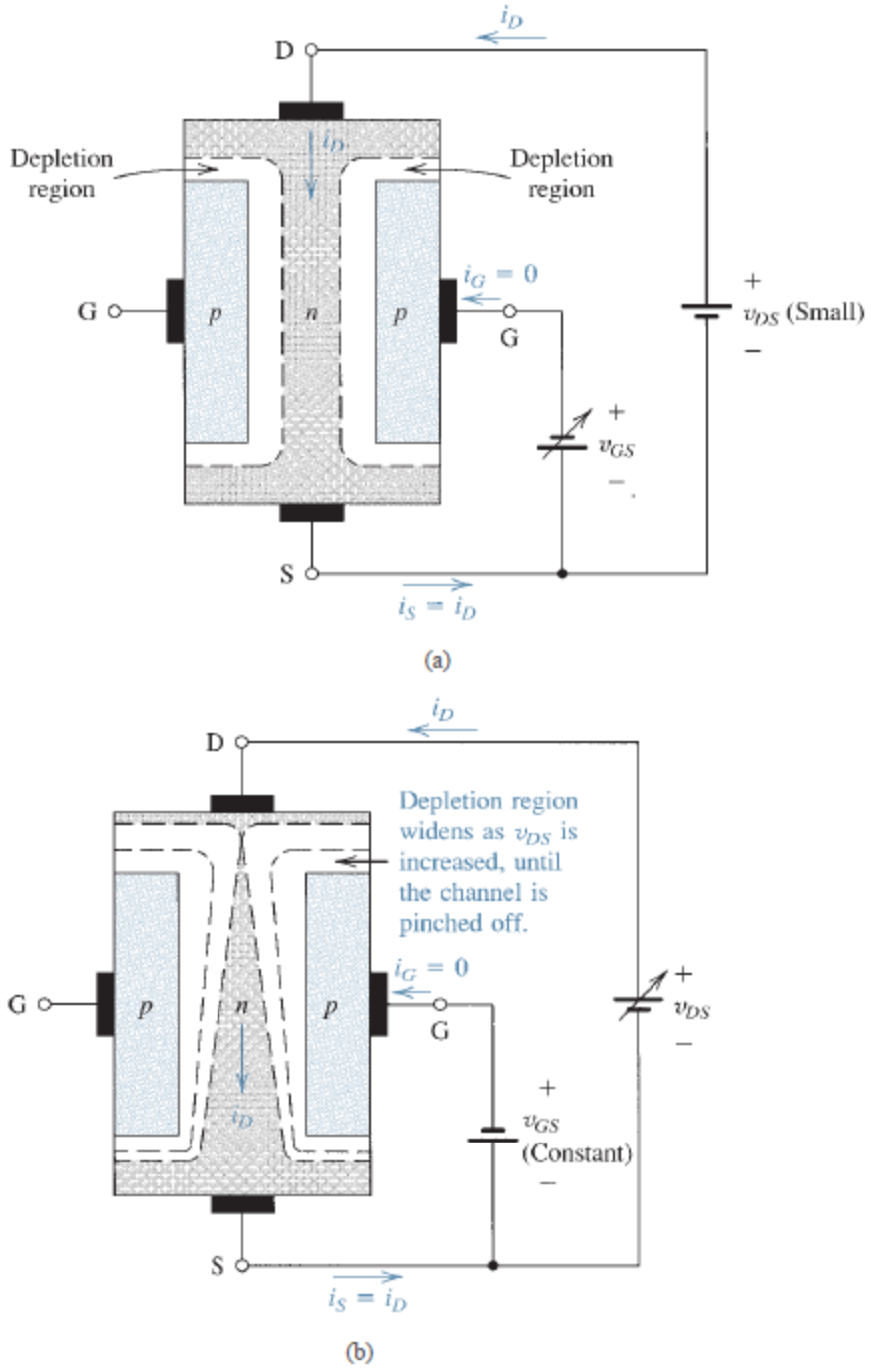


FIGURE x2.2 Physical operation of the *n*-channel JFET: **(a)** For small v_{DS} the channel is uniform and the device functions as a resistance whose value is controlled by v_{GS}. (b) Increasing v_{DS} causes the channel to acquire a tapered shape and eventually pinch-off occurs. Note that, though not shown, the two gate regions are electrically connected.

Consider next the situation shown in Fig. x2.2(b). Here v_{GS} is held constant at a value greater (that is, less negative) than V_P, and v_{DS} is increased. Since v_{DS} appears as a voltage drop across the length of the channel, the voltage increases as we move along the channel from source to drain. It follows that the reverse-bias voltage between gate and channel varies at different points along the channel and is highest at the drain end. Thus the channel acquires a tapered shape and the i_D–v_{DS} characteristic becomes nonlinear. When the reverse bias at the drain end, v_{GD}, falls below the pinch-off voltage V_P, the channel is pinched off at the drain end and the drain current saturates. The remainder of the description of JFET operation follows closely that given for the depletion MOSFET. The description above clearly indicates that the JFET is a depletion-type device. Its characteristics should therefore be similar to those of the depletion-type MOSFET. This is true with a very important exception: While it is possible to operate the depletion-type MOSFET in the enhancement mode (by simply applying a positive v_{GS} if the device is *n* channel) this is impossible in the JFET case. If we attempt to apply a positive v_{GS}, the gate–channel *pn* junction becomes forward biased and the gate ceases to control the channel. Thus the maximum v_{GS} is limited to 0 V, though it is possible to go as high as 0.3 V or so since a *pn* junction remains essentially cut off at such a small forward voltage.

x2.1.3 Current–Voltage Characteristics

The current–voltage characteristics of the JFET are identical to those of the depletion-mode MOSFET studied in Section 5.4.6 of the eighth edition except that for the JFET the maximum v_{GS} allowed is normally 0 V. Furthermore, the JFET is specified in terms of the pinch-off voltage V_P (equal to V_t of the MOSFET) and the *d*rain-to-*s*ource current with the gate *s*horted to the source, I_{DSS}, which corresponds to $\frac{1}{2}k_n V_t^2$ for the MOSFET. With these substitutions, the *n*-channel JFET characteristics can be described as follows:

Cutoff: $v_{GS} \le V_P$, $i_D = 0$

Triode region: $V_P \le v_{GS} \le 0$, $v_{DS} \le v_{GS} - V_P$

$$i_D = I_{DSS}\left[2\left(1 - \frac{v_{GS}}{V_P}\right)\left(\frac{v_{DS}}{V_P}\right) - \left(\frac{v_{DS}}{V_P}\right)^2\right] \tag{x2.1}$$

Saturation (pinch-off) region: $V_P \le v_{GS} \le 0$, $v_{DS} \ge v_{GS} - V_P$

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) \tag{x2.2}$$

where λ is the inverse of the Early voltage; $\lambda = 1/V_A$, and V_A and λ are positive for *n*-channel devices.

Recalling that for an *n*-channel device, V_P is negative, we see that operation in the pinch-off region is obtained when the drain voltage is greater than the gate voltage by at least $|V_P|$.

Since the gate–channel junction is always reverse-biased, only a leakage current flows through the gate terminal. From Chapter 3 of the eighth edition, we know that such a current is of the order of 10^{-9} A. Although i_G is very small, and is assumed zero in almost all applications, it should be noted that the gate current in a JFET is many orders of magnitude greater than the gate current in a MOSFET. Of course the latter is so tiny

because of the insulated gate structure. Another complication arises in the JFET because of the strong dependence of gate leakage current on temperature—approximately doubling for every 10°C rise in temperature, just as in the case of a reverse-biased diode (see Chapter 4).

x2.1.4 The *p*-Channel JFET

The current–voltage characteristics of the *p*-channel JFET are described by the same equations as the *n*-channel JFET. Note, however, that for the *p*-channel JFET, V_P is positive, $0 \le v_{GS} \le V_P$, v_{DS} is negative, λ and V_A are negative, and the current i_D flows out of the drain terminal. To operate the *p*-channel JFET in pinch-off, $v_{DS} \le v_{GS} - V_P$, which in words means that the drain voltage must be lower than the gate voltage by at least $|V_P|$. Otherwise, with $v_{DS} \ge v_{GS} - V_P$, the *p*-channel JFET operates in the triode region.

x2.1.5 The JFET Small-Signal Model

The JFET small-signal model is identical to that of the MOSFET [see Fig. 7.13(b)]. Here, g_m is given by

$$g_m = \left(\frac{2I_{DSS}}{|V_P|}\right)\left(1 - \frac{V_{GS}}{V_P}\right) \tag{x2.3}$$

or alternatively by

$$g_m = \left(\frac{2I_{DSS}}{|V_P|}\right)\sqrt{\frac{I_D}{I_{DSS}}} \tag{x2.4}$$

where V_{GS} and I_D are the dc bias quantities, and

$$r_o = \frac{|V_A|}{I_D} \tag{x2.5}$$

At high frequencies, the equivalent circuit of Fig. 10.4(c) applies with C_{gs} and C_{gd} being both depletion capacitances. Typically, C_{gs} = 1 to 3 pF, C_{gd} = 0.1 to 0.5 pF, and f_T = 20 to 100 MHz.

EXERCISES

In Exercises x2.1 to x2.4, let the *n*-channel JFET have V_P = –4 V and I_{DSS} = 10 mA, and unless otherwise specified assume that in pinch-off (saturation) the output resistance is infinite.

x2.1 For $v_{GS} = -2$ V, find the minimum v_{DS} for the device to operate in pinch-off. Calculate i_D for $v_{GS} = -2$ V and $v_{DS} = 3$ V.

Ans. 2 V; 2.5 mA

x2.2 For $v_{DS} = 3$ V, find the change in i_D corresponding to a change in v_{GS} from −2 to −1.6 V.

Ans. 1.1 mA

x2.3 For small v_{DS}, calculate the value of r_{DS} at $v_{GS} = 0$ V and at $v_{GS} = -3$ V.

Ans. 200 Ω; 800 Ω

x2.4 If $V_A = 100$ V, find the JFET output resistance r_o when operating in pinch-off at a current of 1 mA, 2.5 mA, and 10 mA.

Ans. 100 kΩ; 40 kΩ; 10 kΩ

xD2.5 The JFET in the circuit of Fig. xE2.5 has $V_P = -3$ V, $I_{DSS} = 9$ mA, and $\lambda = 0$. Find the values of all resistors so that $V_G = 5$ V, $I_D = 4$ mA, and $V_D = 11$ V. Design for 0.05 mA in the voltage divider.

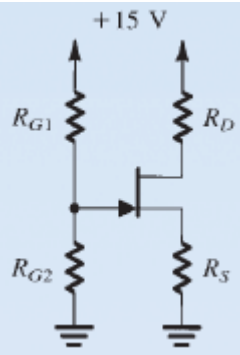


FIGURE xE2.5

Ans. $R_{G1} = 200$ kΩ; $R_{G2} = 100$ kΩ; $R_S = 1.5$ kΩ; $R_D = 1$ kΩ

x2.6 For the JFET circuit designed in Exercise x2.5, let an input signal v_i be capacitively coupled to the gate, a large bypass capacitor be connected between the source and ground, and the output signal v_o be taken from the drain through a large coupling capacitor. The resulting common-source amplifier is shown in Fig. xE2.6. Calculate g_m and r_o (assuming $V_A = 100$ V). Also find R_i, $A_v \equiv (v_o/v_i)$, and R_o.

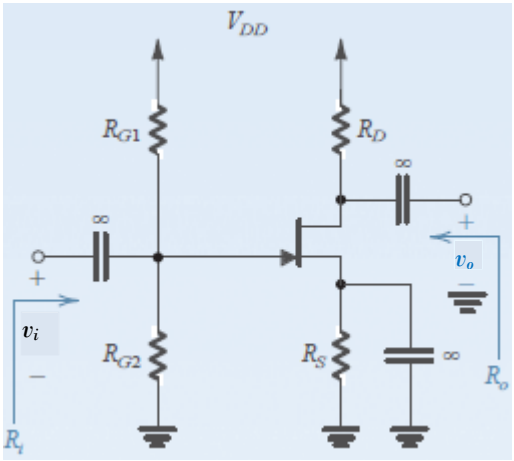


FIGURE xE2.6

Ans. 4 mA/V; 25 kΩ; 66.7 kΩ; −3.8 V/V; 962 Ω

x2.2 Gallium Arsenide Devices: The MESFET

The devices discussed thus far, and indeed the devices used in most of the circuits studied in this book, are made of silicon. This reflects the situation that has existed in the microelectronics industry for at least five decades. Furthermore, owing to the advances that are continually being made in silicon device and circuit technologies, the dominance of silicon as the most useful semiconductor material is expected to continue for many years to come. Nevertheless, another semiconductor material has been making inroads into digital applications that require extremely high speeds of operation and analog applications that require very high operating frequencies. We refer to gallium arsenide (GaAs), a compound semiconductor formed of gallium, which is in the third column of the periodic table of elements, and arsenic, which is in the fifth column; thus GaAs is known as a III-V semiconductor.

The major advantage that GaAs offers over silicon is that electrons travel much faster in *n*-type GaAs than in silicon. This is a result of the fact that the electron drift mobility μ_n (which is the constant that relates the electron drift velocity to the electric field; velocity = $\mu_n E$) is five to ten times higher in GaAs than in silicon. Thus for the same input voltages, GaAs devices have higher output currents, and thus higher g_m, than the corresponding silicon devices. The larger output currents enable faster charging and discharging of load and parasitic capacitances and thus result in increased speeds of operation.

Gallium arsenide devices have been used for some years in the design of discrete component amplifiers for microwave applications (in the 10^9 Hz or GHz frequency range). More recently, GaAs has begun to be employed in the design of very-high-speed digital integrated circuits and in analog ICs, such as op amps, that operate in the hundreds of MHz frequency range. Although the technology is still relatively immature, suffering from yield and reliability problems and generally limited to low levels of integration, it offers great potential. Therefore, this book includes a brief study of GaAs devices and circuits. Specifically, the basic GaAs devices are studied in this section; their basic amplifier circuit configurations are discussed in Section x2.3 of this supplement; and GaAs digital circuits are studied in Section x2.4.

x2.2.1 The Basic GaAs Devices

Although there are a number of GaAs technologies currently in various stages of development, we shall study the most mature of these technologies. The active device available in this technology is an *n*-channel field effect transistor known as the **metal semiconductor FET** or **MESFET.** The technology also provides a type of diode known as the **Schottky barrier diode (SBD).** (The SBD is briefly introduced in Section x8.3.1 of the bonus material.) The structure of these two basic devices is illustrated by their cross sections, depicted in Fig. x2.3. The GaAs circuit is formed on an undoped GaAs substrate. Since the conductivity of undoped GaAs is very low, the substrate is said to be semi-insulating. This turns out to be an advantage for GaAs technology as it simplifies the process of isolating the devices on the chip from one another, as well as resulting in smaller parasitic capacitances between the devices and the circuit ground.

As indicated in Fig. x2.3, a Schottky-barrier diode consists of a metal–semiconductor junction. The metal, referred to as the Schottky-barrier metal to distinguish it from the different kind of metal used to make a contact (see Long and Butner (1990) for a detailed explanation of the difference), forms the anode of the diode. The *n*-type GaAs forms the cathode. Note that heavily doped *n*-type GaAs (indicated by n^+) is used between the *n* region and the cathode metal contact in order to keep the parasitic series resistance low.

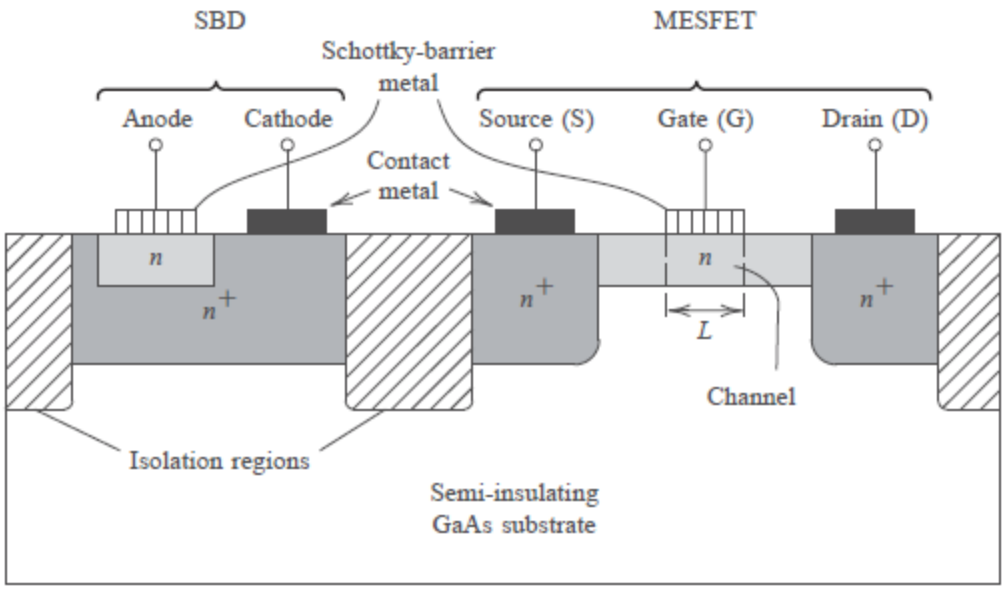


FIGURE x2.3 Cross-section of a GaAs Schottky-barrier diode (SBD) and a MESFET.

The gate of the MESFET is formed by Schottky-barrier metal in direct contact with the *n*-type GaAs that forms the channel region. The channel length L is defined by the length of the gate electrode, and similarly for the width W (in the direction perpendicular to the page). To reduce the parasitic resistances between the drain and source contacts and the channel, the two contacts are surrounded with heavily doped (n^+) GaAs.

Since the main reason for using GaAs circuits is to achieve high speed/frequency of operation, the channel length is made as small as possible. Typically, L = 0.2 to 2.0 μm. Also, usually all the transistors on the IC chip are made to have the same length, leaving only the width W of each device to be specified by the circuit designer.

Only *n*-channel MESFETs are available in GaAs technology. This is because holes have a relatively low drift mobility in GaAs, making *p*-channel MESFETs unattractive. The lack of complementary transistors is a definite disadvantage of GaAs technology. Correspondingly, it makes the task of the circuit designer even more challenging than usual.

x2.2.2 Device Operation

The MESFET operates in a very similar manner to the JFET, with the Schottky metal playing the role of the *p*-type gate of the JFET (refer to Fig. x2.1). Basically, a depletion region forms in the channel below the gate surface, and the thickness of the depletion region is controlled by the gate voltage v_{GS}. This in turn effects control over the channel dimensions and thus on the current that flows from drain to source in response to an applied v_{DS}. The latter voltage causes the channel to have a tapered shape, with pinch-off eventually occurring at the drain end of the channel.

The most common GaAs MESFETs available are of the depletion type with a threshold voltage V_t (or, equivalently, pinch-off voltage V_P) in the range of −0.5 to −2.5 V. These devices can be operated with v_{GS} values ranging from the negative V_t to positive values as high as a few tenths of a volt. However, as v_{GS} reaches 0.7 V or so, the Schottky-barrier diode between gate and channel conducts heavily and the gate voltage no longer effectively controls the drain-to-source current. Gate conduction, which is not possible in MOSFETs, is another definite disadvantage of the MESFET.

Although less common, enhancement-mode MESFETs are available in certain technologies. These normally-off devices are obtained by arranging that the depletion region existing at $v_{GS} = 0$ extends through the entire channel depth, thus blocking the channel and causing $i_D = 0$. To cause current to flow from drain to source the channel must be opened by applying to the gate a positive voltage of sufficient magnitude to reduce the thickness of the depletion region below that of the channel region. Typically, the threshold voltage V_t is between 0.1 and 0.3 V.

The above description of MESFET operation suggests that the i_D–v_{DS} characteristics should saturate at $v_{DS} = v_{GS} - V_t$, as is the case in a silicon JFET. It has been observed, however, that the i_D–v_{DS} characteristics of GaAs MESFETs saturate at lower values of v_{DS} and, furthermore, that the saturation voltages v_{DSsat} do not depend strongly on the value of v_{GS}. This "early saturation" phenomenon comes about because the velocity of the electrons in the channel does not remain proportional to the electric field (which in turn is determined by v_{DS} and L; $E = v_{DS}/L$) as is the case in silicon; rather, the electron velocity reaches a high peak value and then saturates (that is, becomes constant independent of v_{DS}). The velocity saturation effect is even more pronounced in short-channel devices ($L \leq 1$ μm), occurring at values of v_{DS} lower than $(v_{GS} - V_t)$.

Finally, a few words about the operation of the Schottky-barrier diode. Forward current is conducted by the majority carriers (electrons) flowing into the Schottky-barrier metal (the anode). Unlike the *pn*-junction diode, minority carriers play no role in the operation of the SBD. As a result, the SBD does not exhibit minority-carrier storage effects, which give rise to the diffusion capacitance of the *pn*-junction diode. Thus, the SBD has only one capacitive effect, associated with the depletion-layer capacitance C_j.

x2.2.3 Device Characteristics and Models

A first-order model for the MESFET, suitable for hand calculations, is obtained by neglecting the velocity-saturation effect, and thus the resulting model is almost identical to that of the JFET though expressed somewhat differently in order to correspond to the literature:

$$i_D = 0 \qquad \text{for } v_{GS} < V_t \tag{x2.6}$$

$$i_D = \beta\,[2(v_{GS} - V_t)\,v_{DS} - v_{DS}^2]\,(1 + \lambda v_{DS}) \qquad \text{for } v_{GS} \geq V_t,\ v_{DS} < v_{GS} - V_t \tag{x2.7}$$

$$i_D = \beta\,(v_{GS} - V_t)^2\,(1 + \lambda v_{DS}) \qquad \text{for for } v_{GS} \geq V_t,\ v_{DS} \geq v_{GS} - V_t \tag{x2.8}$$

The only differences between these equations and those for the JFETs are: (1) the channel-length modulation factor, $1 + \lambda v_{DS}$, is included also in the equation describing the triode region (also called the ohmic region) simply because λ of the MESFET is rather large and including this factor results in a better fit to measured characteristics; and (2) a transconductance parameter β is used so as to correspond with the MESFET literature. Obviously, β is related to I_{DSS} of the JFET and $k'(W/L)$ of the MOSFET. (Note, however, that this β has absolutely nothing to do with β of the BJT!)

A modification of this model to account for the early saturation effects is given in Hodges and Jackson (1988).

Figure x2.4(a) shows the circuit symbol for the depletion-type *n*-channel GaAs MESFET. Since only one type of transistor (*n* channel) is available, all devices will be

drawn the same way, and there should be no confusion as to which terminal is the drain and which is the source.

The circuit symbol of the Schottky-barrier diode is depicted in Fig. x2.4(b). In spite of the fact that the physical operation of the SBD differs from that of the *pn*-junction diode, their i–v characteristics are identical. Thus the i–v characteristic of the SBD is given by the same exponential relationship studied in Chapter 4. For the GaAs SBD, the constant[1] n is typically in the range of 1 to 1.2.

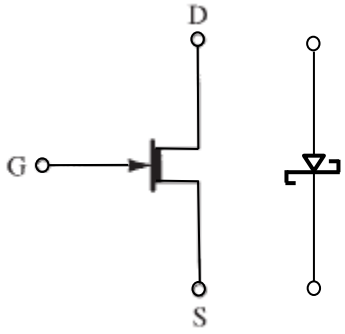
The small-signal model of the MESFET is identical to that of other FET types. The parameter values are given by

$$g_m = 2\beta(V_{GS} - V_t)(1 + \lambda V_{DS}) \tag{x2.9}$$

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1} = 1/\lambda\beta(V_{GS} - V_t)^2 \tag{x2.10}$$

The MESFET, however, has a rather high value for λ (0.1 to 0.3 V^{-1}) which results in a small output resistance r_o. This turns out to be a serious drawback of GaAs MESFET technology, resulting in low voltage-gain obtainable from each stage. Furthermore, it has been found that r_o decreases at high frequencies. Circuit design techniques for coping with the low r_o will be presented in Section x2.3 of this supplement.

For easy reference, Table x2.1 gives typical values for device parameters in a GaAs MESFET technology. The devices in this technology have a channel length $L = 1$ μm. The values given are for a device with a width $W = 1$ μm. The parameter values for actual devices can be obtained by appropriately scaling by the width W. This process is illustrated in the following example. Unless otherwise specified, the values of Table x2.1 are to be used for the exercises and the end-of-chapter problems.



(a) (b)

Figure x2.4 Circuit symbols for (a) an *n*-channel depletion-type GaAs MESFET, and (b) a Schottky-barrier diode (SBD).

[1] The exponential relationship is generally written as $i = I_S e^{v/nV_T}$, where n is a constant that is approximately equal to one for silicon diodes.

Table x2.1	Typical Parameter Values for GaAs MESFETs and Schottky Diodes in L = 1 µm Technology, Normalized for W = 1 µm
$V_t = -1.0$ V	
$\beta = 10^{-4}$ A/V^2	
$\lambda = 0.1$ V^{-1}	
$I_S = 10^{-15}$ A	
$n = 1.1$	

Example x2.1

Figure x2.5 shows a simple GaAs MESFET amplifier, with the W values of the transistors indicated. Assume that the dc component of v_I, that is V_{GS1}, biases Q_1 at the current provided by the current source Q_2 so that both devices operate in saturation and that the dc output is at half of the supply voltage. Find:

(a) the β values for Q_1 and Q_2;

(b) V_{GS1};

(c) g_{m1}, r_{o1}, and r_{o2}; and

(d) the small-signal voltage gain.

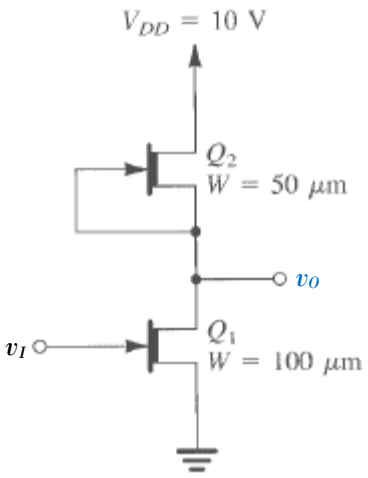


Figure x2.5 Circuit for Example x2.1: A MESFET amplifier.

Solution

(a) The values of β can be obtained by scaling the value given in Table x2.1 using the specified values of W,

$$\beta_1 = 100 \times 10^{-4} = 10^{-2} \text{ A/V}^2 = 10 \text{ mA/V}^2$$

$$\beta_2 = 50 \times 10^{-4} = 5 \times 10^{-3} \text{ A/V}^2 = 5 \text{ mA/V}^2$$

(b)

$$I_{D2} = \beta_2(V_{GS2} - V_t)^2(1 + \lambda V_{DS2})$$
$$= 5(0 + 1)^2(1 + 0.1 \times 5)$$
$$= 7.5 \text{ mA}$$
$$I_{D1} = I_{D2} = 7.5 \text{ mA}$$
$$7.5 = \beta_1(V_{GS1} - V_t)^2(1 + \lambda V_{DS1})$$
$$= 10(V_{GS1} + 1)^2(1 + 0.1 \times 5)$$

Thus,

$$V_{GS1} = -0.3 \text{ V}$$

(c)

$$g_{m1} = 2 \times 10(-0.3 + 1)(1 + 0.1 \times 5)$$
$$= 21 \text{ mA/V}$$
$$r_{o1} = \frac{1}{0.1 \times 10(-0.3 + 1)^2} = 2 \text{ k}\Omega$$
$$r_{o2} = \frac{1}{0.1 \times 5(0 + 1)^2} = 2 \text{ k}\Omega$$

(d)

$$A_v = -g_{m1}(r_{o1} /\!/ r_{o2})$$
$$= -21 \times (2 /\!/ 2) = -21 \text{ V/V}$$

EXERCISE

x2.7 For a MESFET with the gate shorted to the source and having $W = 10$ μm, find the minimum voltage between drain and source to operate in saturation. For $V_{DS} = 5$ V, find the current I_D. What is the output resistance of this current source?

Ans. 1 V; 1.5 mA; 10 kΩ

As already mentioned, the main reason for using GaAs devices and circuits is their high frequency and high speed of operation. A remark is therefore in order on the internal capacitances and f_T of GaAs transistors. For a particular GaAs technology with $L = 1$ μm, C_{gs} (at $V_{GS} = 0$ V) is 1.6 fF/μm-width, and C_{gd} (at $V_{DS} = 2$ V) is 0.16 fF/μm-width. Thus for a MESFET with $W = 100$ μm, $C_{gs} = 0.16$ pF and $C_{gd} = 0.016$ pF. f_T typically ranges from 5 to 15 GHz.

x2.3 Gallium Arsenide Amplifiers

Gallium arsenide (GaAs) technology makes possible the design of amplifiers having very wide bandwidths, in the hundreds of megahertz or even gigahertz range. In this section we shall study some of the circuit design techniques that have been developed over the years for the design of GaAs amplifiers. As will be seen, these techniques aim to circumvent the major problem of the MESFET, namely, its low output resistance in saturation.

x2.3.1 Current Sources

Current sources play a fundamental role in the design of integrated-circuit amplifiers, being employed both for biasing and as active loads. In GaAs technology, the simplest way to implement a current source is to connect the gate of a depletion-type MESFET to its source, as shown in Fig. x2.6(a). Provided that v_{DS} is maintained greater than $|V_t|$, the MESFET will operate in saturation and the current i_D will be

$$i_D = \beta V_t^2 (1 + \lambda v_{DS})$$

Thus the current source will have the equivalent circuit shown in Fig. x2.6(b), where the output resistance is the MESFET r_o,

$$r_o = 1/\lambda\beta V_t^2 \tag{x2.11}$$

In JFET terminology, $\beta V_t^2 = I_{DSS}$ and $\lambda = 1/|V_A|$; thus

$$r_o = |V_A|/I_{DSS} \tag{x2.12}$$

Since for the MESFET, λ is relatively high (0.1 to 0.3 V^{-1}) the output resistance of the current source of Fig. x2.6(a) is usually low, rendering this current-source realization inadequate for most applications. Before considering means for increasing the effective output resistance of the current source, we show in Fig. x2.6(c) how the basic current source can be connected to *source* currents to a load whose voltage can be as high as $V_{DD} - |V_t|$. Alternatively, the same device can be connected as shown in Fig. x2.6(d) to *sink* currents from a load whose voltage can be as low as $-V_{SS} + |V_t|$.

EXERCISE

x2.8 Using the device data given in Table x2.1, find the current provided by a 10-μm-wide MESFET connected in the current-source configuration. Let the source be connected to a −5-V supply and find the current when the drain voltage is −4V. What is the output resistance of the current source? What change in current occurs if the drain voltage is raised by +4V?

Ans. 1.1 mA; 10 kΩ; 0.4 mA

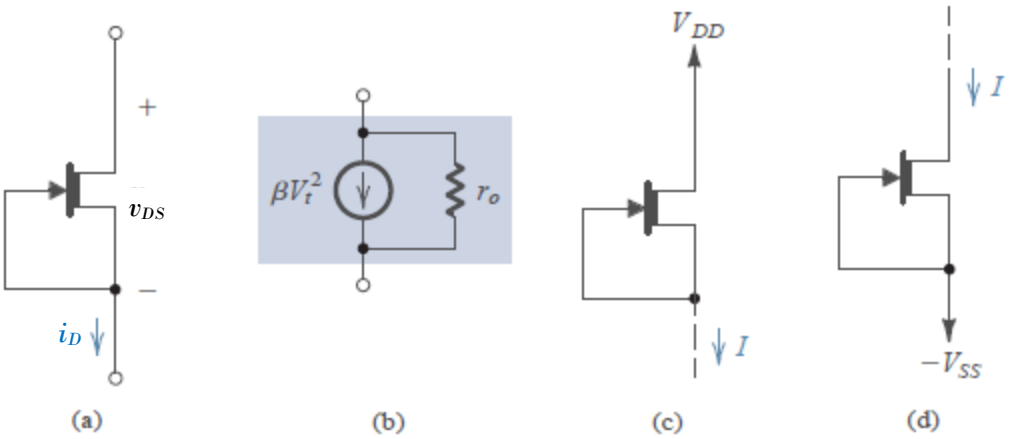


FIGURE x2.6 **(a)** The basic MESFET current source; **(b)** equivalent circuit of the current source; **(c)** the current source connected to a positive power supply to source currents to loads at voltages $\leq V_{DD} - |V_t|$; **(d)** the current source connected to a negative power supply to sink currents from loads at voltages $\geq -V_{SS} + |V_t|$.

x2.3.2 A Cascode Current Source

The output resistance of the current source can be increased by utilizing the cascode configuration as shown in Fig. x2.7. The output resistance R_o of the cascode current source can be found by using Eq. (8.73) from the textbook,

$$R_o \simeq g_{m2} r_{o2} r_{o1}$$

Thus, adding the cascode transistor Q_2 raises the output resistance of the current source by the factor $g_{m2}r_{o2}$, which is the intrinsic voltage gain of Q_2. For GaAs MESFETs, $g_{m2}r_{o2}$ is typically 10 to 40. To allow a wide range of voltages at the output of the cascode current source, V_{BIAS} should be the lowest value that results in Q_1 operating in saturation.

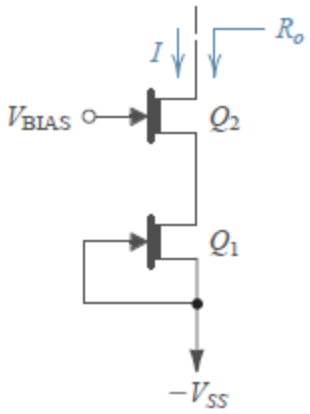


FIGURE x2.7 Adding the cascode transistor Q_2 increases the output resistance of the current source by the factor $g_{m2}r_{o2}$; that is, $R_o = g_{m2}r_{o2}r_{o1}$.

EXERCISE

xD2.9 For the cascode current source of Fig. x2.7 let V_{SS} = 5 V, W_1 = 10 μm, and W_2 = 20 μm, and assume that the devices have the typical parameter values given in Table x2.1. (a) Find the value of V_{BIAS} that will result in Q_1 operating at the edge of the saturation region (i.e., $V_{DS1} = |V_t|$) when the voltage at the output is −3 V. (b) What is the lowest allowable voltage at the current-source output? (c) What value of output current is obtained for V_O = −3 V? (d) What is the output resistance of the current source? (e) What change in output current results when the output voltage is raised from −3 V to +1 V?

Ans. (a) −4.3 V; (b) −3.3 V; (c) 1.1 mA; (d) 310 kΩ; (e) 0.013 mA

x2.3.3 Increasing the Output Resistance by Bootstrapping

Another technique frequently employed to increase the effective output resistance of a MESFET, including the current-source-connected MESFET, is known as **bootstrapping.** The bootstrapping idea is illustrated in Fig. x2.8(a). Here the circuit inside the box senses the voltage at the bottom node of the current source, v_A, and causes a voltage v_B to appear at the top node of a value

$$v_B = V_S + \alpha v_A \tag{x2.13}$$

where V_S is the dc voltage required to operate the current-source transistor in saturation, and α is a constant ≤1.

The incremental output resistance of the bootstrapped current source can be found by causing the voltage v_A to increase by an increment v_a. From Eq. (x2.13) we find that the resulting increment in v_B is $v_b = \alpha v_a$. The incremental current through the current source is therefore $(v_a - v_b)/r_o$ or $(1 - \alpha)\, v_a/r_o$. Thus the output resistance R_o is

$$R_o = \frac{v_a}{(1-\alpha)\, v_a/r_o} = \frac{r_o}{1-\alpha} \tag{x2.14}$$

Thus, bootstrapping increases the output resistance by the factor $1/(1 - \alpha)$, which increases as α approaches unity. Perfect bootstrapping is achieved with $\alpha = 1$, resulting in $R_o = \infty$. From the above we observe that the bootstrapping circuit senses whatever change occurs in the voltage at one terminal of the current source and causes an almost equal change to occur at the other terminal, thus maintaining an almost constant voltage across the current source and thus minimizing the change in current through the current-source transistor. The action of the bootstrapping circuit can be likened to that of a person who attempts to lift himself off the ground by pulling on the straps of his boots (!), the origin of the name of this circuit technique, which, incidentally, predates GaAs technology. Bootstrapping is a form of positive feedback; the signal v_b that is fed back by the bootstrapping circuit is in phase with (has the same polarity as) the signal that is being sensed, v_a. Feedback will be studied formally in Chapter 11.

An implementation of the bootstrapped current source is shown in Fig. x2.8(b). Here transistor Q_2 is a source follower used to buffer node A, whose voltage is being sensed. The width of Q_2 is half that of Q_1 and is operating at half the bias current. (Transistors Q_1 and Q_2 are said to operate at the same **current density.**) Thus V_{GS} of Q_2 will be equal to

that of Q_1—namely, zero—and hence $V_C = V_A$. The two Schottky diodes behave as a battery of approximately 1.4 V, resulting in the dc voltage at node E being 1.4 V higher than V_C. Note that the signal voltage at node C appears intact at node E; only the dc level is shifted. The diodes are said to perform **level shifting,** a common application of Schottky diodes in GaAs MESFET technology.

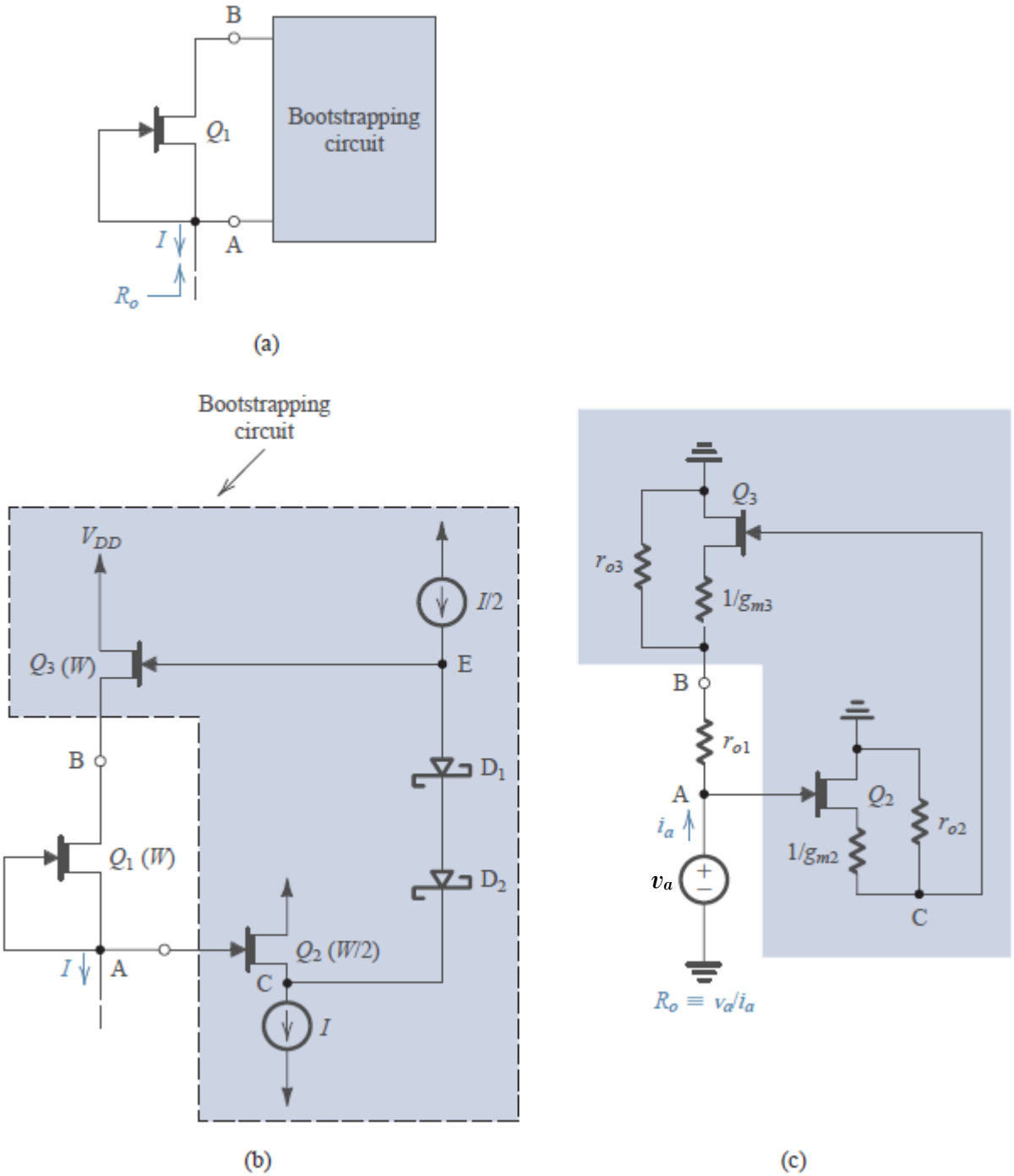


FIGURE x2.8 Bootstrapping of a MESFET current source Q_1: **(a)** basic arrangement; **(b)** an implementation; **(c)** small-signal equivalent circuit model of the circuit in (b), for the purpose of determining the output resistance R_o.

Transistor Q_3 is a source follower that is operating at the same current density as Q_1, and thus its V_{GS} must be zero, resulting in $V_B = V_E$. The end result is that the bootstrapping circuit causes a dc voltage of 1.4 V to appear across the current-source transistor Q_1. Provided that $|V_t|$ of Q_1 is less than 1.4 V, Q_1 will be operating in saturation as required.

To determine the output resistance of the bootstrapped current source, we apply an incremental voltage v_a to node A, as shown in Fig. x2.8(c). Note that this small-signal equivalent circuit is obtained by implicitly using the T model (including r_o) for each FET and assuming that the Schottky diodes act as a perfect level shifter (that is, as an ideal dc voltage of 1.4 V with zero internal resistance). Analysis of this circuit is straightforward and yields

$$\alpha \equiv \frac{v_b}{v_a} = \frac{g_{m3}r_{o3}\dfrac{g_{m2}r_{o2}}{g_{m2}r_{o2}+1} + \dfrac{r_{o3}}{r_{o1}}}{g_{m3}r_{o3} + \dfrac{r_{o3}}{r_{o1}} + 1}$$

which is smaller than, but close to, unity, as required. The output resistance R_o is then obtained as

$$\begin{aligned} R_o &\equiv \frac{v_a}{i_a} = \frac{r_{o1}}{1-\alpha} \\ &= r_{o1}\frac{g_{m3}r_{o3} + \left({}^{r_{o3}}/_{r_{o1}}\right) + 1}{g_{m3}r_{o3}/(g_{m2}r_{o2}+1) + 1} \end{aligned} \tag{x2.15}$$

For $r_{o3} = r_{o1}$, assuming that $g_{m3}r_{o3}$ and $g_{m2}r_{o2}$ are $\gg 1$, and using the relationships for g_m and r_o for Q_2 and Q_3, one can show that

$$R_o \simeq r_{o1}\,(g_{m3}r_{o3}/2) \tag{x2.16}$$

which represents an increase of about an order of magnitude in output resistance. Unfortunately, however, the circuit is rather complex.

x2.3.4 A Simple Cascode Configuration–The Composite Transistor

The rather low output resistance of the MESFET places a severe limitation on the performance of MESFET current sources and various MESFET amplifiers. This problem can be alleviated by using the composite MESFET configuration shown in Fig. x2.9(a) in place of a single MESFET. This circuit is unique to GaAs MESFETs and works only because of the early-saturation phenomenon observed in these devices. Recall from the discussion in Section x2.1 that **early saturation** refers to the fact that in a GaAs MESFET the drain current saturates at a voltage $v_{DS\,\text{sat}}$ that is lower than $v_{GS} - V_t$.

In the composite MESFET of Fig. x2.9(a), Q_2 is made much wider than Q_1. It follows that since the two devices are conducting the same current, Q_2 will have a gate-to-source voltage v_{GS2} whose magnitude is much closer to $|V_t|$ than $|v_{GS1}|$ is (thus, $|v_{GS2}| \gg |v_{GS1}|$). For instance, if we use the devices whose typical parameters are given in Table x2.1 and ignore for the moment channel-length modulation ($\lambda = 0$), we find that for $W_1 = 10$ μm and $W_2 = 90$ μm, at a current of 1 mA, $v_{GS1} = 0$ and $v_{GS2} = -\frac{2}{3}$ V. Now, since the drain-to-source voltage of Q_1 is $v_{DS1} = -v_{GS2} + v_{GS1}$, we see that v_{DS1} will be positive and close to but

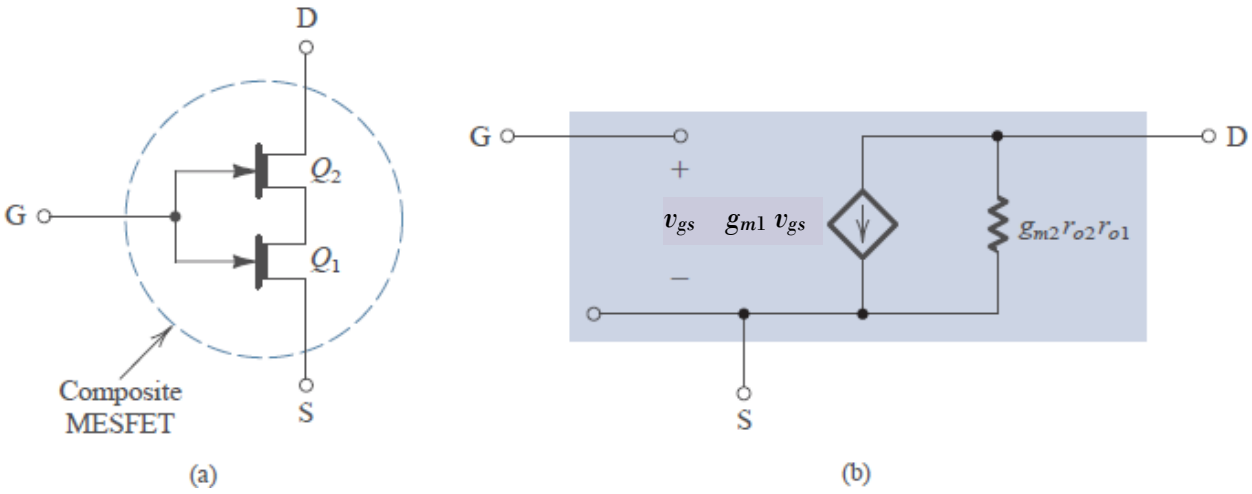


FIGURE x2.9 (**a**) The composite MESFET and (**b**) its small-signal model.

lower than $v_{GS1} - V_t$ (⅔ V in our example compared to 1 V). Thus in the absence of early saturation, Q_1 would be operating in the triode region. With early saturation, however, saturation-mode operation is achieved for Q_1 by making Q_2 5 to 10 times wider.

The composite MESFET of Fig. x2.9(a) can be thought of as a cascode configuration, in which Q_2 is the cascode transistor, but without a separate bias line to feed the gate of the cascode transistor (as in Fig. x2.7). By replacing each of Q_1 and Q_2 with their small-signal models one can show that the composite device can be represented with the equivalent circuit model of Fig. x2.9(b). Thus while g_m of the composite device is equal to that of Q_1, the output resistance is increased by the intrinsic gain of Q_2, $g_{m2}r_{o2}$, which is typically in the range 10 to 40. This is a substantial increase and is the reason for the attractiveness of the composite MESFET.

The composite MESFET can be employed in any of the applications that can benefit from its increased output resistance. Some examples are shown in Fig. x2.10. The circuit in Fig. x2.10(a) is that of a current source with increased output resistance. Another view of the operation of this circuit can be obtained by considering Q_2 as a source follower that causes the drain of Q_1 to follow the voltage changes at the current-source terminal (node A), thereby bootstrapping Q_1 and increasing the effective output resistance of the current source. This alternative interpretation of circuit operation has resulted in its alternative name: the **self-bootstrapped** current source.

The application of the composite MESFET as a source follower is shown in Fig. x2.10(b). Assuming the bias-current source I to be ideal, we can write for the gain of this follower

$$\frac{v_o}{v_i} = \frac{r_{o,\text{eff}}}{r_{o,\text{eff}} + (1/g_{m1})} = \frac{g_{m2}r_{o2}r_{o1}}{g_{m2}r_{o2}r_{o1} + (1/g_{m1})} \tag{x2.17}$$

which is much closer to the ideal value of unity than is the gain of a single MESFET source follower.

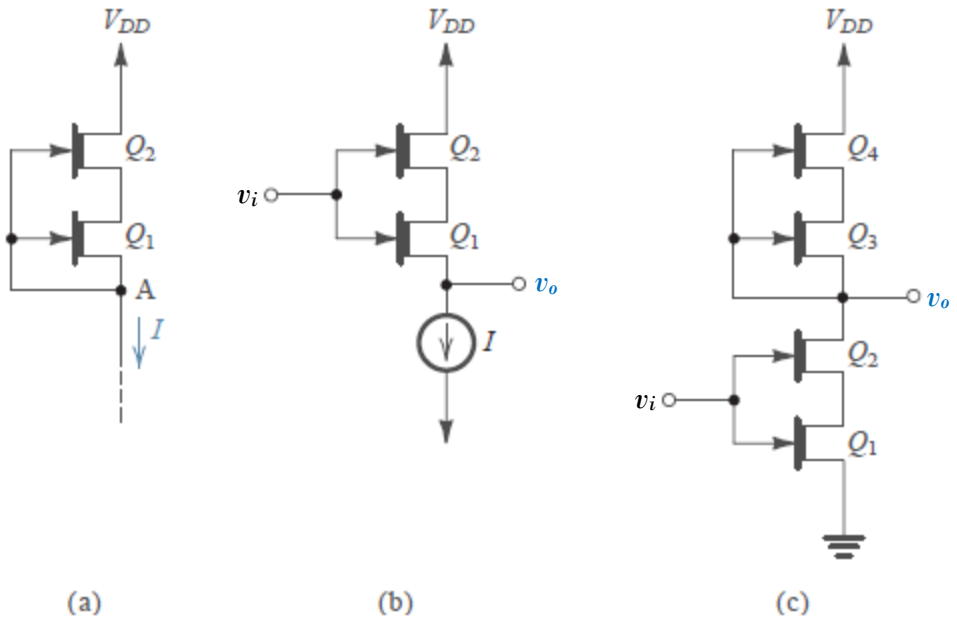


FIGURE x2.10 Applications of the composite MESFET: **(a)** as a current source; **(b)** as a source follower; and **(c)** as a gain stage.

EXERCISE

x2.10 Using the device data given in Table x2.1, contrast the voltage gain of a source follower formed using a single MESFET having $W = 10$ μm with a composite MESFET follower with $W_1 = 10$ μm and $W_2 = 90$ μm. In both cases assume biasing at 1 mA and neglect λ while calculating g_m (for simplicity).

Ans. Single: 0.952 V/V; composite: 0.999 V/V

A final example of the application of the composite MESFET is shown in Fig. x2.10(c). The circuit is a gain stage utilizing a composite MESFET (Q_1, Q_2) as a driver and another composite MESFET (Q_3, Q_4) as a current-source load. The small-signal gain is given by

$$\frac{v_o}{v_i} = -g_{m1}R_o \tag{x2.18}$$

where R_o is the output resistance,

$$\begin{aligned} R_o &= r_{o,\text{eff}}(Q_1, Q_2)//r_{o,\text{eff}}(Q_3, Q_4) \\ &= g_{m2}r_{o2}r_{o1}//g_{m4}r_{o4}r_{o3} \end{aligned} \tag{x2.19}$$

x2.3.5 Differential Amplifiers

The simplest possible implementation of a differential amplifier in GaAs MESFET technology is shown in Fig. x2.11. Here Q_1 and Q_2 form the differential pair, Q_3 forms the bias current source, and Q_4 forms the active (current-source) load. The performance of the circuit is impaired by the low output resistances of Q_3 and Q_4. The voltage gain is given by

$$\frac{v_o}{v_i} = -g_{m2}(r_{o2}//r_{o4}) \tag{x2.20}$$

The gain can be increased by using one of the improved current-source implementations discussed above. Also, a rather ingenious technique has been developed for enhancing the gain of the MESFET differential pair. The circuit is shown in Fig. x2.12(a). While the drain of Q_2 is loaded with a current-source load (as before), the output signal developed is fed back to the drain of Q_1 via the source follower Q_3. The small-signal analysis of the circuit is illustrated in Fig. x2.12(b) where the current sources I and $I/2$ have been assumed ideal and thus replaced with open circuits. To determine the voltage gain, we have grounded the gate terminal of Q_2 and applied the differential input signal v_i to the gate of Q_1. The analysis proceeds along the following steps:

1. From the output node we see that $i_{d2} = 0$.
2. From the sources node, since $i_{d2} = 0$, we find that $i_{d1} = 0$.
3. From the node at the drain of Q_1, since $i_{d1} = 0$, we find that $i_{d3} = 0$.
4. Writing for each transistor

$$i_d = g_m v_{gs} + (v_{ds}/r_o) = 0$$

we obtain three equations in the three unknowns v_{d1}, v_s, and v_o. The solution yields

$$\frac{v_o}{v_i} = g_{m1}r_{o1}/\left[\frac{g_{m1}r_{o1}+1}{g_{m2}r_{o2}+1} - \frac{g_{m3}r_{o3}}{g_{m3}r_{o3}+1}\right] \tag{x2.21}$$

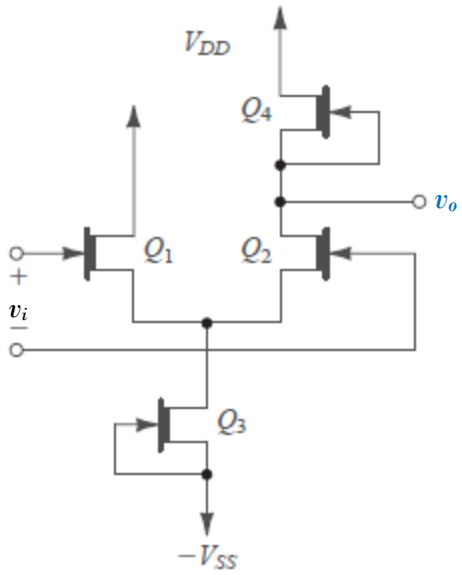


FIGURE x2.11 A simple MESFET differential amplifier.

If all three transistors have the same geometry and are operating at equal dc currents, their g_m and r_o values will be equal and the expression in Eq. (x2.21) reduces to

$$\frac{v_o}{v_i} \simeq (g_m r_o)^2$$

Thus application of positive feedback through follower Q_3 enables one to obtain a gain equal to the square of that naturally available from a single stage!

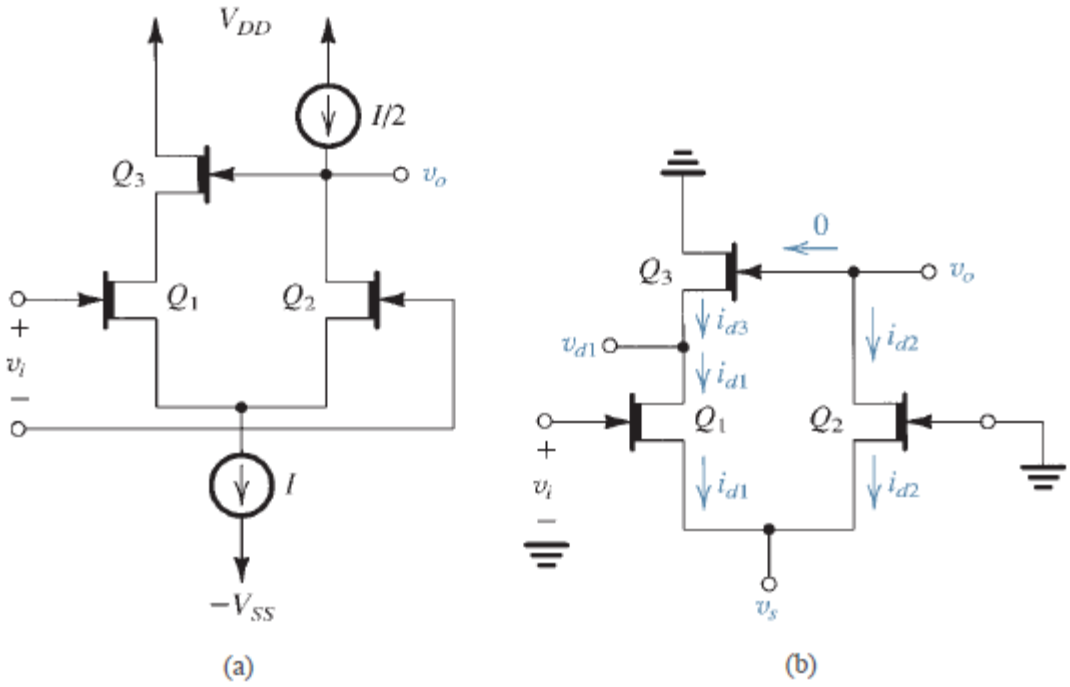


FIGURE x2.12 **(a)** A MESFET differential amplifier whose gain is enhanced by the application of positive feedback through the source follower Q_3; **(b)** small-signal analysis of the circuit in (a).

EXERCISE

x2.11 Using the device data given in Table x2.1, find the gain of the differential amplifier circuit of Fig. x2.12(a) for I = 10 mA and $W_1 = W_2 = W_3$ = 100 μm.

Ans. 784 V/V

x2.4 Gallium Arsenide Digital Circuits

In this section we study logic circuits implemented using gallium arsenide devices. The major advantage that GaAs technology offers is a higher speed of operation than can be achieved using silicon devices. The disadvantages are a relatively high power dissipation per gate (1 to 10 mW); relatively small voltage swings and, correspondingly, narrow noise margins; low packing density, mostly as a result of the high-power dissipation per

gate; and low manufacturing yield. The present state of affairs is that a few specialized manufacturers produce SSI, MSI, and some LSI digital circuits performing relatively specialized functions, with a cost per gate considerably higher than that of silicon digital ICs. Nevertheless, the very high speeds of operation achievable in GaAs circuits make it a worthwhile technology whose applications will possibly grow.

Unlike the CMOS logic circuits that are studied in Chapter 16 and the bipolar logic families that are presented in Supplement x8 of the bonus materials, there are no standard GaAs logic-circuit families. The lack of standards extends not only to the topology of the basic gates but also to the power-supply voltages used. In the following we present examples of the most popular GaAs logic gate circuits.

x2.4.1 Direct-Coupled FET Logic (DCFL)

Direct-coupled FET logic (DCFL) is the simplest form of GaAs digital logic circuits. The basic gate is shown in Fig. x2.13. The gate utilizes enhancement MESFETs, Q_1 and Q_2, for the input switching transistors, and a depletion MESFET for the load transistor Q_L. The gate closely resembles the now obsolete depletion-load MOSFET circuit. The GaAs circuit of Fig. x2.13 implements a two-input NOR function.

To see how the MESFET circuit of Fig. x2.13 operates, ignore input B and consider the basic inverter formed by Q_1 and Q_L. When the input voltage applied to node A, v_I, is lower than the threshold voltage of the enhancement MESFET Q_1, denoted V_{tE}, transistor Q_1 will be off. Recall that V_{tE} is positive and for GaAs MESFETs is typically 0.1 to 0.3 V. Now if the gate output Y is open circuited, the output voltage will be very close to V_{DD}. In practice, however, the gate will be driving another gate, as indicated in Fig. x2.13, where Q_3 is the input transistor of the subsequent gate. In such a case, current will flow from V_{DD} through Q_L and into the gate terminal of Q_3. Recalling that the gate to source of a GaAs MESFET is a Schottky-barrier diode that exhibits a voltage drop of about 0.7 V when conducting, we see that the gate conduction of Q_3 will clamp the output high voltage (V_{OH}) to about 0.7 V. This is in sharp contrast to the MOSFET case, where no gate conduction takes place.

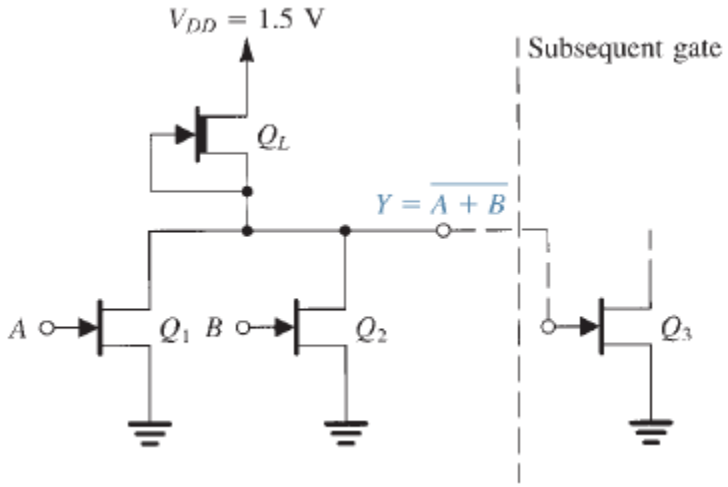


FIGURE x2.13 A DCFL GaAs gate implementing a two-input NOR function. The gate is shown driving the input transistor Q_3 of another gate.

Figure x2.14 shows the DCFL inverter under study with the input of the subsequent gate represented by a Schottky diode Q_3. With $v_I < V_{tE}$, $i_1 = 0$ and i_L flows through Q_3 resulting in $v_O = V_{OH} \simeq 0.7$ V. Since V_{DD} is usually low (1.2 to 1.5 V) and the threshold voltage of Q_L, V_{tD}, is typically −0.7 to −1 V, Q_L will be operating in the triode region. (To simplify matters, we shall ignore in this discussion the early-saturation effect exhibited by GaAs MESFETs.) As v_I is increased above V_{tE}, Q_1 turns on and conducts a current denoted i_1. Initially, Q_1 will be in the saturation region. Current i_1 subtracts from i_L, thus reducing the current in Q_3. The voltage across Q_3, v_O, decreases slightly. However, for the present discussion we shall assume that v_O will remain close to 0.7 V as long as Q_3 is conducting. This will continue until v_I reaches the value that results in $i_1 = i_L$. At this point, Q_3 ceases conduction and can be ignored altogether. Further increase in v_I results in i_1 increasing, v_O decreasing, and $i_L = i_1$. When $(V_{DD} - v_O)$ exceeds $|V_{tD}|$, Q_L saturates; and when v_O falls below v_I by V_{tE}, Q_1 enters the triode region. Eventually, when $v_I = V_{OH} = 0.7$ V, $v_O = V_{OL}$, which is typically 0.1 to 0.2 V.

From the description above we see that the output voltage swing of the DCFL gate is limited by gate conduction to a value less than 0.7 V (typically 0.5 V or so). Further details on the operation of the DCFL gate are illustrated by the following example.

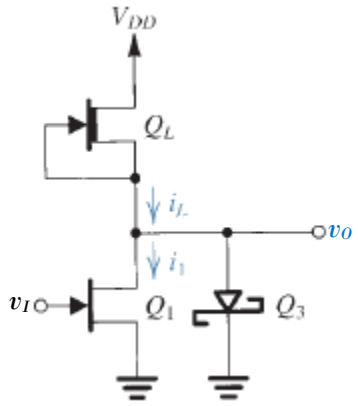


FIGURE x2.14 The DCFL gate with the input of the subsequent gate represented by a Schottky diode Q_3.

Example x2.2

Consider a DCFL gate fabricated in a GaAs technology for which $L = 1$ μm, $V_{tD} = -1$ V, $V_{tE} = 0.2$ V, β (for 1-μm width) $= 10^{-4}$ A/V^2, and $\lambda = 0.1$ V^{-1}. Let the widths of the input MESFETs be 50 μm, and let the width of the load MESFET be 6 μm. $V_{DD} = 1.5$ V. Using a constant-voltage drop model for the gate-source Schottky diode with $V_D = 0.7$ V, and neglecting the early saturation effect of GaAs MESFETs (that is, using Eqs. x2.6–x2.8 to describe MESFET operation), find V_{OH}, V_{OL}, V_{IH}, NM_H, NM_L, the static power dissipation, and the propagation delay for a total equivalent capacitance at the gate output of 30 fF.

Solution

From the description above of the operation of the DCFL gate we found that $V_{OH} = 0.7$ V. To obtain V_{OL}, we consider the inverter in the circuit of Fig. x2.14 and let $v_I = V_{OH} = 0.7$ V. Since we expect $v_O = V_{OL}$ to be small, we assume Q_1 to be in the triode region and Q_L to be in saturation. (Q_3 is of course off.) Equating i_1 and i_L gives the equation

$$\beta_1 [2 (0.7 - 0.2) V_{OL} - V^2_{OL}] (1 + 0.1 V_{OL}) = \beta_L [0 - (-1)]^2 [1 + 0.1 (1.5 - V_{OL})]$$

To simplify matters, we neglect the terms $0.1V_{OL}$ and substitute $\beta_L / \beta_1 = W_L / W_1 = 6 / 50$ to obtain a quadratic equation in V_{OL} whose solution gives $V_{OL} \simeq 0.17$ V.

Toward obtaining the value of V_{IL} we shall first find the value of v_I at which $i_1 = i_L$, the diode Q_3 turns off, and v_O begins to decrease. Since at this point $v_O = 0.7$ V, we assume that Q_1 is in saturation. Transistor Q_L has a v_{DS} of 0.8 V, which is less than $|V_{tD}|$ and is thus in the triode region. Equating i_1 and i_L gives

$$\beta_1 (v_I - 0.2)^2 (1 + 0.1 \times 0.7) = \beta_L [2 (1) (1.5 - 0.7) - (1.5 - 0.7)^2] [1 + 0.1 (1.5 - 0.7)]$$

Substituting $\beta_L / \beta_1 = W_L / W_1 = 6 / 50$ and solving the resulting equation yields $v_I = 0.54$ V. Figure x2.15 shows a sketch of the transfer characteristic of the inverter. The slope dv_O / dv_I at point A can be found to be −14.2 V/V. We shall consider point A as the point at which the inverter begins to switch from the high-output state; thus $V_{IL} \simeq 0.54$ V.

To obtain V_{IH}, we find the co-ordinates of point B at which $dv_O / dv_I = -1$. This can be done using a procedure similar to that employed for the MOSFET inverters and assuming Q_1 to be in the triode region and Q_L to be in saturation. Neglecting terms in $0.1v_O$, the result is $V_{IH} \simeq 0.63$ V. The noise margins can now be found as

$$NM_H \equiv V_{OH} - V_{IH} = 0.7 - 0.63 = 0.07 \text{ V}$$

$$NM_L \equiv V_{IL} - V_{OL} = 0.54 - 0.17 = 0.37 \text{ V}$$

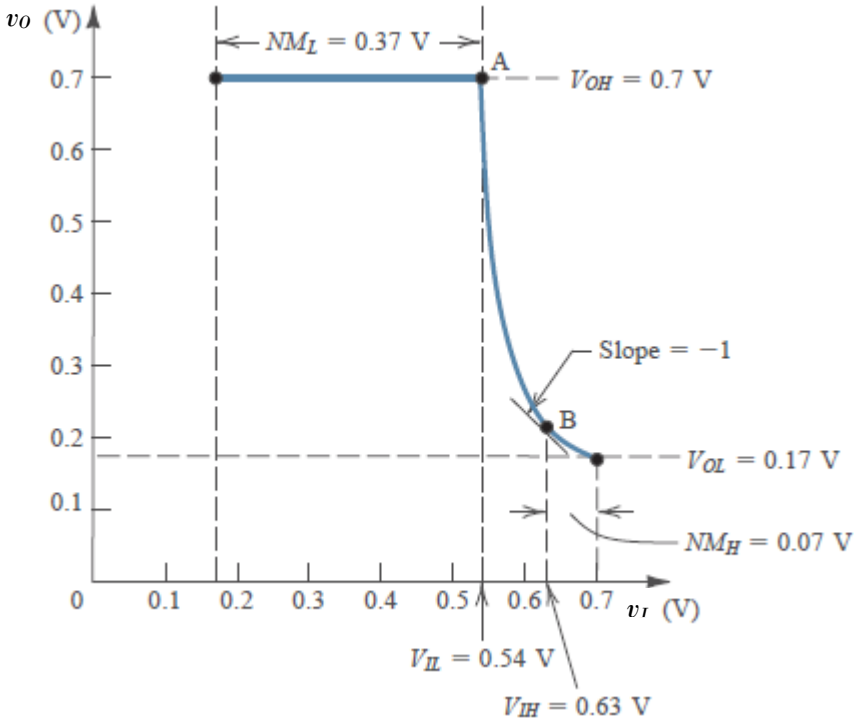


FIGURE x2.15 Transfer characteristic of the DCFL inverter of Fig. x2.14.

The static power dissipation is determined by finding the supply current I_{DD} in the output high and the output-low cases. When the output is high (at 0.7 V), Q_L is in the triode region and the supply current is

$$I_{DD} = \beta_L [2 (0 + 1) (1.5 – 0.7) – (1.5 – 0.7)^2] [1 + 0.1 (1.5 – 0.7)]$$

Substituting $\beta_L = 10^{-4} \times W_L = 0.6$ mA/V^2 results in

$$I_{DD} = 0.61 \text{ mA}$$

When the output is low (at 0.17 V), Q_L is in saturation and the supply current is

$$I_{DD} = \beta_L(0 + 1)^2 [1 + 0.1(1.5 – 0.17)] = 0.68 \text{ mA}$$

Thus the average supply current is

$$I_{DD} = ½(0.61 + 0.68) = 0.645 \text{ mA}$$

and the static power dissipation is

$$P_D = 0.645 \times 1.5 \simeq 1 \text{ mW}$$

The propagation delay t_{PHL} is the time for the output voltage of the inverter to decrease from $V_{OH} = 0.7$ V to $½(V_{OH} + V_{OL}) = 0.435$ V. During this time v_I is at the high level of 0.7 V, and the capacitance C (assumed to be 30 fempto Farads [fF]) is discharged by $(i_1 - i_L)$; refer to Fig. x2.16(a). The average discharge current is found by calculating i_1 and i_L at the beginning and at the end of the discharge interval. The result is that i_1 changes from 1.34 mA to 1.28 mA and i_L changes from 0.61 mA to 0.66 mA. Thus the discharge current $(i_1 - i_L)$ changes from 0.73 mA to 0.62 mA for an average value of 0.675 mA. Thus

$$t_{PHL} = \frac{C\Delta V}{I} = \frac{30 \times 10^{-15}(0.7 - 0.435)}{0.675 \times 10^{-3}} = 11.8 \text{ ps}$$

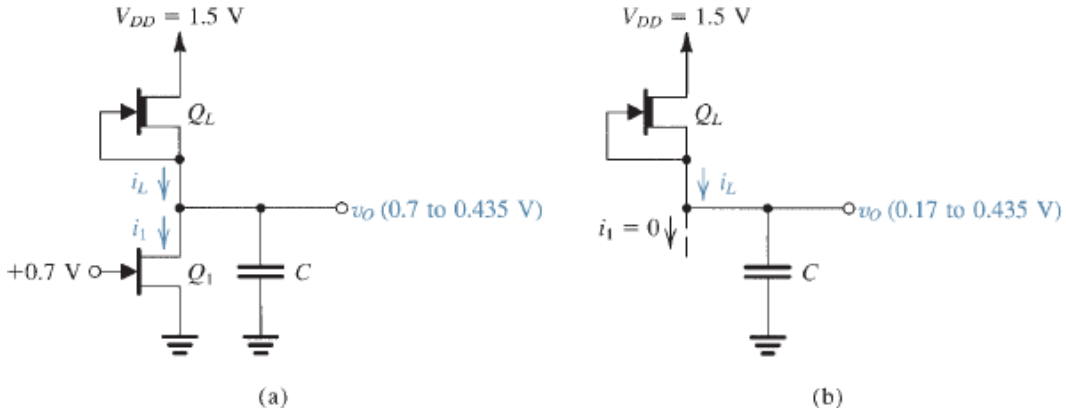


FIGURE x2.16 Circuits for calculating the propagation delays of the DCFL inverter: **(a)** t_{PHL}; **(b)** t_{PLH}.

To determine t_{PLH} we refer to the circuit in Fig. x2.16(b) and note that during t_{PLH}, v_O changes from $V_{OL} = 0.17$ V to $\frac{1}{2}(V_{OH} + V_{OL}) = 0.435$ V. The charging current is the average value of i_L, which changes from 0.8 mA to 0.66 mA. Thus $i_{L|\text{average}} = 0.73$ mA and

$$t_{PHL} = \frac{30 \times 10^{-15} \times (0.435 - 0.17)}{0.73 \times 10^{-3}} = 10.9 \text{ ps}$$

The propagation delay of the DCFL gate can now be found as

$$t_P = \tfrac{1}{2}(t_{PHL} + t_{PLH}) = 11.4 \text{ ps}$$

As a final remark, we note that the analysis above was done using simplified device models; our objective is to show how the circuit works rather than to find accurate performance measures. These can be obtained using SPICE simulation with more elaborate models.

x2.4.2 Logic Gates Using Depletion MESFETs

The DCFL circuits studied above require both enhancement and depletion devices and thus are somewhat difficult to fabricate. Also, owing to the fact that the voltage swings and noise margins are rather small, very careful control of the value of V_{tE} is required in fabrication. As an alternative, we now present circuits that utilize depletion devices only.

Figure x2.17 shows the basic inverter circuit of a family of GaAs logic circuits known at FET logic (FL). The heart of the FL inverter is formed by the switching transistor Q_S and its load Q_L—both depletion-type MESFETs. Since the threshold voltage of a depletion MESFET, V_{tD}, is negative, a negative voltage $< V_{tD}$ is needed to turn Q_S off. On the other hand the output low voltage at the drain of Q_S will always be positive. It follows that the logic levels at the drain of Q_S are not compatible with the levels required at the gate input. The incompatibility problem is solved by simply shifting the level of the voltage down by two diode drops, that is, by approximately 1.4 V. This level shifting is accomplished by the two Schottky diodes D_1 and D_2. The depletion transistor Q_{PD} provides a constant-current bias for D_1 and D_2. To ensure that Q_{PD} operates in the saturation region at all times, its source is connected to a negative supply $-V_{SS}$, and the value of V_{SS} is selected to be equal to or greater than the lowest level of $v_O(V_{OL})$ plus the magnitude of the threshold voltage, $|V_{tD}|$. Transistor Q_{PD} also supplies the current required to discharge a load capacitance when the output voltage of the gate goes low, hence the name "pull-down" transistor and the subscript *PD*.

To see how the inverter of Fig. x2.17 operates, refer to its transfer characteristic, shown in Fig. x2.18. The circuit is usually designed using MESFETs having equal channel lengths (typically 1 μm) and having widths $W_S = W_L = 2W_{PD}$. The transfer characteristic shown is for the case $V_{tD} = -0.9$ V. For v_I lower than V_{tD}, Q_S will be off and Q_L will operate in saturation, supplying a constant current I_L to D_1 and D_2. Transistor Q_{PD} will also operate in saturation with a constant current $I_{PD} = \frac{1}{2}I_L$. The difference between the two currents will flow through the gate terminal of the input transistor of the next gate in the chain, Q_{S2}. Thus the input Schottky diode of Q_{S2} clamps the output voltage v_O to

approximately 0.7 V, which is the output high level, V_{OH}. (Note that for this discussion we shall neglect the finite output resistance in saturation.)

As v_I is raised above V_{tD}, Q_S turns on. Since its drain is at +2.1 V, Q_S will operate in the saturation region and will take away some of the current supplied by Q_L. Thus the current flowing into the gate of Q_{S2} decreases by an equal amount. If we keep increasing v_I, a value is reached for which the current in Q_S equals ½I_L, thus leaving no current to flow through the gate of Q_{S2}. This corresponds to the point labeled A on the transfer characteristic. A further slight increase in v_I will cause the voltage to fall to the point B where Q_S enters the triode region. The segment AB of the transfer curve represents the high-gain region of operation, having a slope equal to $-g_{ms}R$ where R denotes the total equivalent resistance at the drain node. Note that this segment is shown as vertical in Fig. x2.18 because we are neglecting the output resistance in saturation.

The segment BC of the transfer curve corresponds to Q_S operating in the triode region. Here Q_L and Q_{PD} continue to operate in saturation and D_1 and D_2 remain conducting. Finally, for $v_I = V_{OH} = 0.7$ V, $v_O = V_{OL}$, which for the case $V_{tD} = -0.9$ V is −1.3 V.

EXERCISE

x2.12 Verify that the coordinates of points A, B, and C of the transfer characteristic are as indicated in Fig. x2.18. Let $V_{tD} = -0.9$ V and $\lambda = 0$.

As indicated in Fig. x2.18, the FL inverter exhibits much higher noise margins than those for the DCFL circuit. The FL inverter, however, requires two power supplies.

The FL inverter can be used to construct a NOR gate by simply adding transistors with drain and source connected in parallel with those of Q_S.

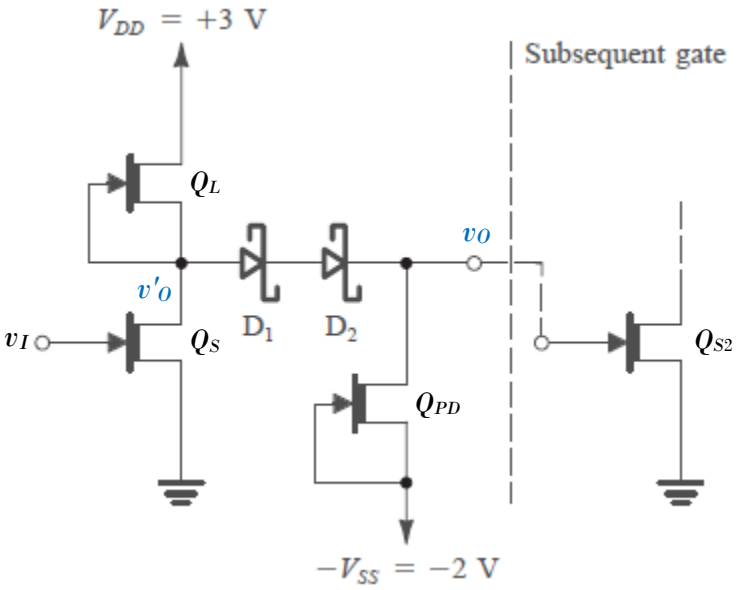


FIGURE x2.17 An inverter circuit utilizing depletion-mode devices only. Schottky diodes are employed to shift the output logic levels to values compatible with the input levels required to turn the depletion MESFET Q_S on and off. This circuit is known as FET logic (FL).

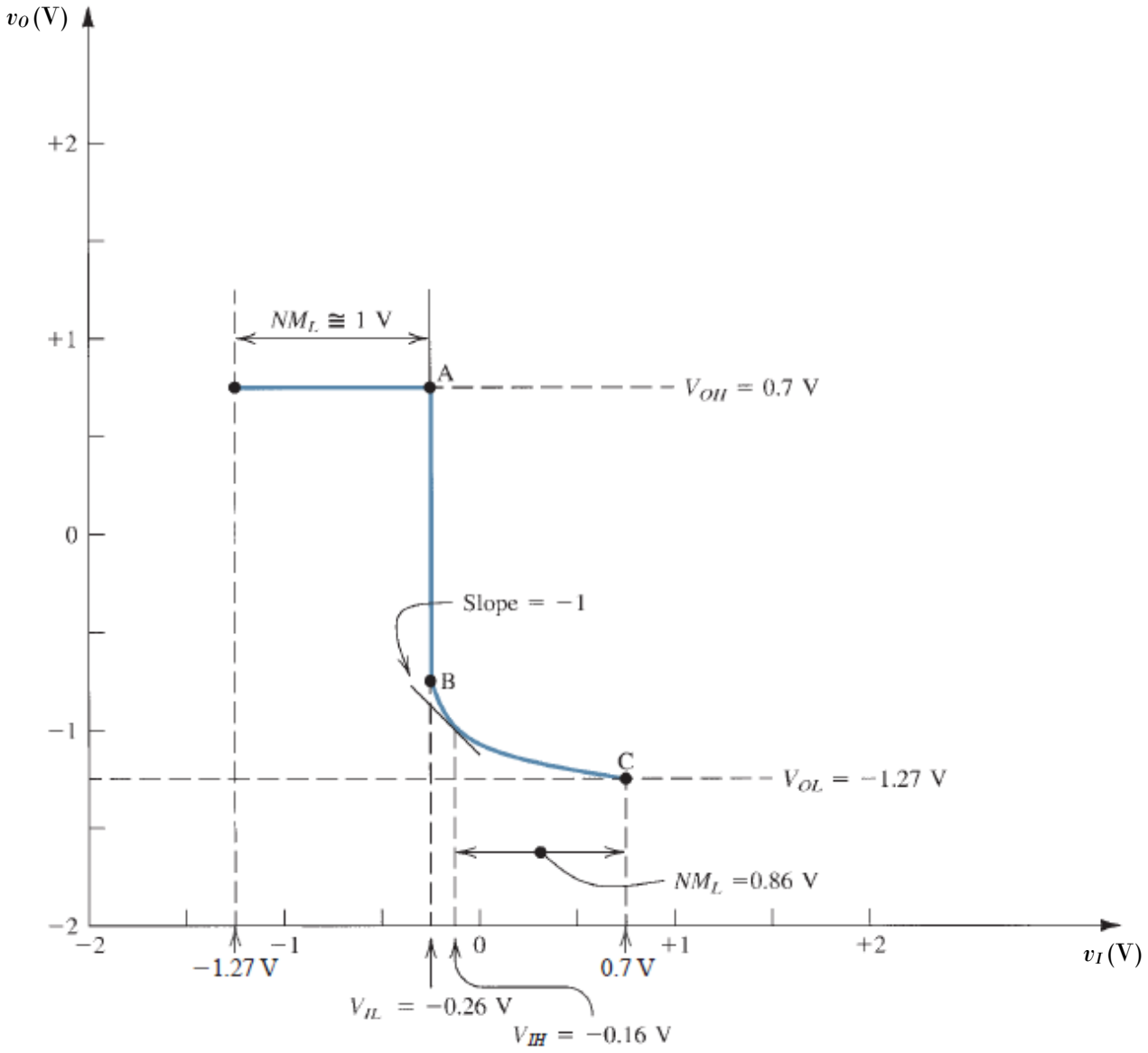


FIGURE x2.18 Transfer characteristic of the FL inverter of Fig. x2.17.

x2.4.3 Schottky Diode FET Logic (SDFL)

If the diode level-shifting network of the FL inverter is connected at the input side of the gate, rather than at the output side, we obtain the circuit shown in Fig. x2.19(a). This inverter operates in much the same manner as the FL inverter. The modified circuit, however, has a very interesting feature: The NOR function can be implemented by simply connecting additional diodes, as shown in Fig. x2.19(b). This logic form is known as Schottky diode FET logic (SDFL). SDFL permits higher packing density than other forms of MESFET logic because only an additional diode, rather than an additional transistor, is required for each additional input, and diodes require much smaller areas than transistors.

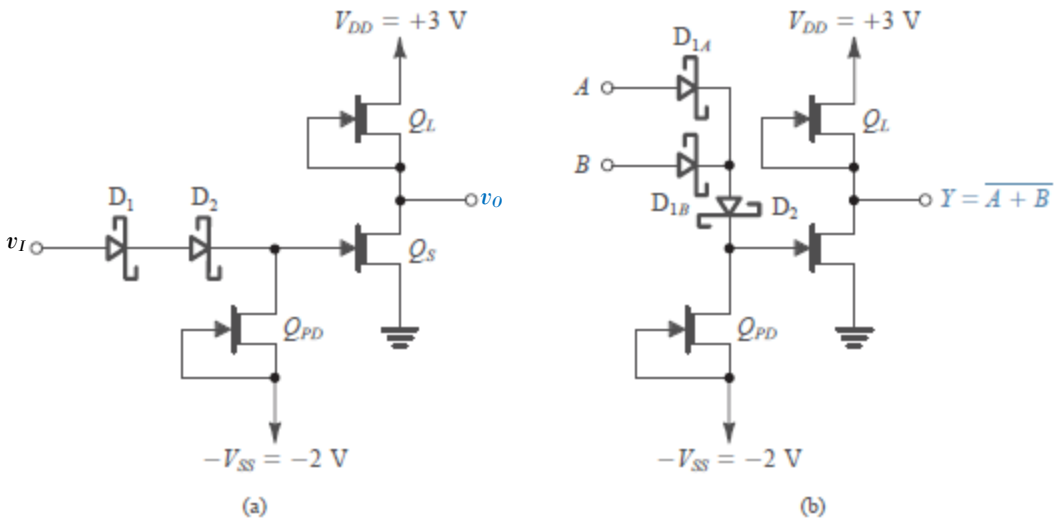


FIGURE x2.19 **(a)** An SDFL inverter. **(b)** An SDFL NOR gate.

x2.4.4 Buffered FET Logic (BFL)

Another variation on the basic FL inverter of Fig. x2.17 is possible. A source follower can be inserted between the drain of Q_S and the diode level-shifting network. The resulting gate, shown for the case of a two-input NOR, is depicted in Fig. x2.20. This form of GaAs logic circuit is known as buffered FET logic (BFL). The source-follower transistor Q_{SF} increases the output current-driving capability, thus decreasing the low-to-high propagation time. FL, BFL, and SDFL feature propagation delays of the order of 100 ps and power dissipation of the order of 10 mW/gate.

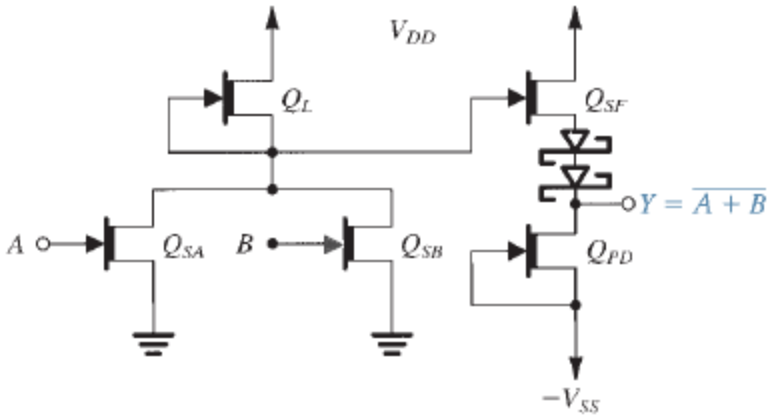


FIGURE x2.20 A BFL two-input NOR gate. The gate is formed by inserting a source-follower transistor Q_{SF} between the inverting stage and the level-shifting stage.