

# Microelectronic Circuits

## 8<sup>th</sup> Edition

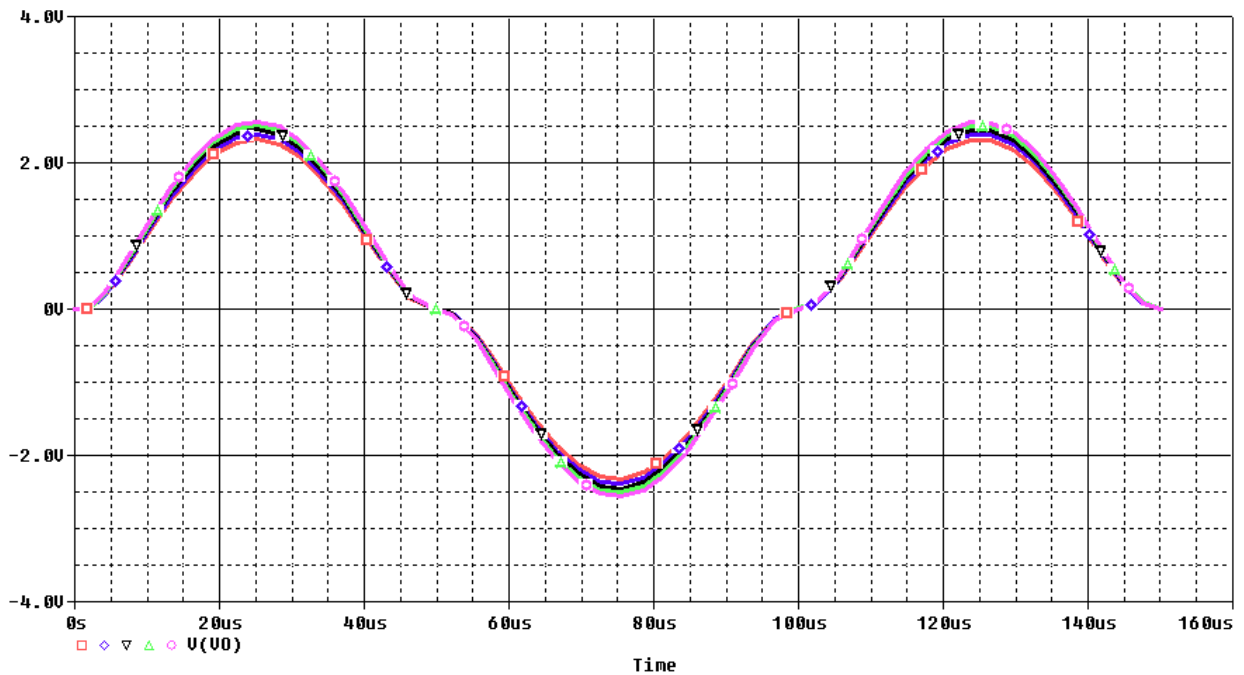
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*Spice Problems Solutions*  
*Chapter 12*

*Prepared by: Nijwm Wary*  
*2019*



4. The cross over interval is  $2 \times 2.9 \mu\text{s} = 5.8 \mu\text{s}$ . So, it is 5.8 %.
5. Run the parametric analysis and sweep RL from  $500 \Omega$  to  $700 \Omega$  in steps of  $50 \Omega$  or smaller. Plot  $V(\text{VO})$  as shown below.



6. The output voltage is half of the input voltage when  $R_L = 650 \Omega$ .

### Netlist:

Copy the netlist given below and paste it into a text file and save it with \*.cir extension.

```

*****Problem: P12_12 *****
***** Main circuit begins here*****
V_DD      VDD 0 5Vdc
V1        VIN 0
+SIN 0 5 10k 0 0 0
R1        0 VO {RL}
V_SS     0 VSS 5Vdc
M2        VSS VIN VO VO PMOS0P5
+ L=0.5u
+ W=10u
+ M=1
M1        VDD VIN VO VO NMOS0P5
+ L=0.5u
+ W=5u
+ M=1
.PARAM   r1=1MEG
***** Main circuit ends here*****

```

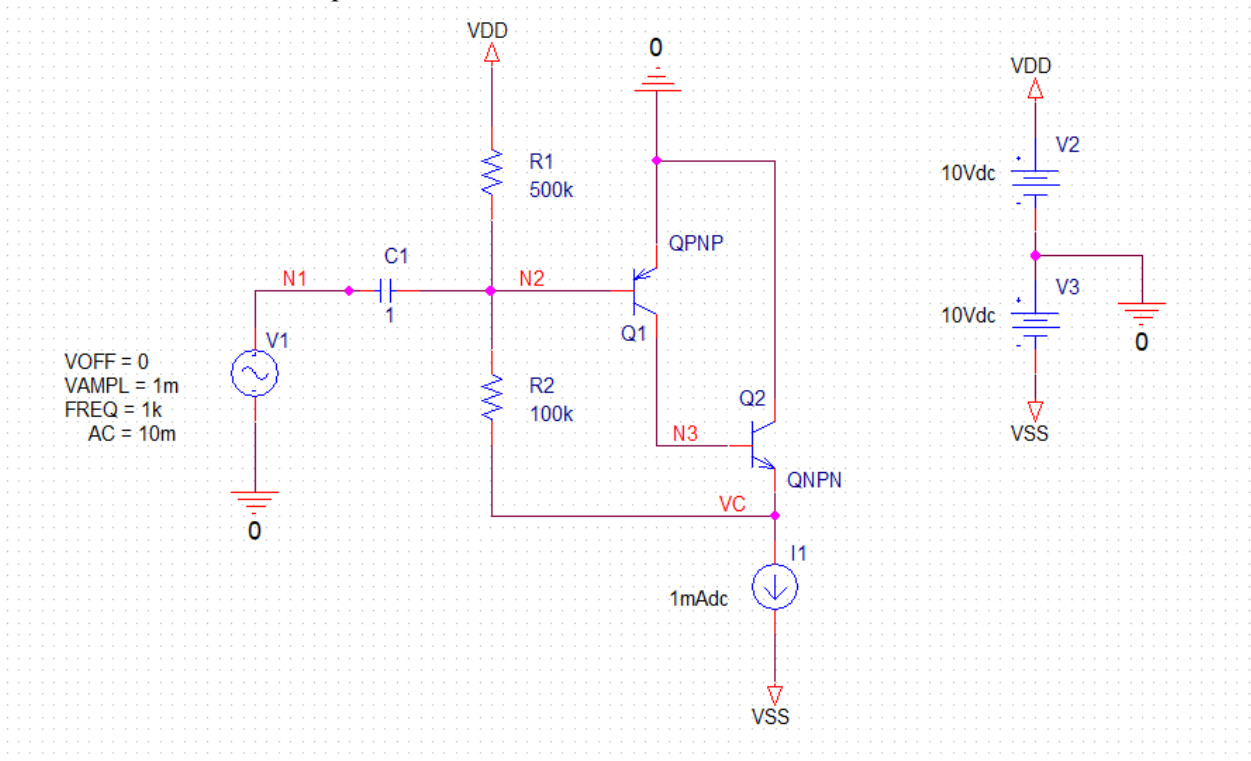
```
***** NMOS and PMOS models begins here *****
.model NMOS0P5    NMOS(Level=1 VTO=0.5 GAMMA=0.5 PHI=0.8
+                LD=0 WD=0 UO=550 LAMBDA=0 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+                CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+                CGSO=0.4E-9)

.model PMOS0P5    PMOS(Level=1 VTO=-0.5 GAMMA=0.45 PHI=0.8
+                LD=0 WD=0 UO=275 LAMBDA=0 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+                CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+                CGSO=0.35E-9)
***** NMOS and PMOS model ends here *****

***** Analysis begins here*****
.TRAN          10uS  0.15mS
*.STEP        LIN          PARAM          RL          500  700  50
.PROBE
.END
***** Analysis ends here*****
```

**Problem: 12.39**

7. The schematic for this problem is shown below



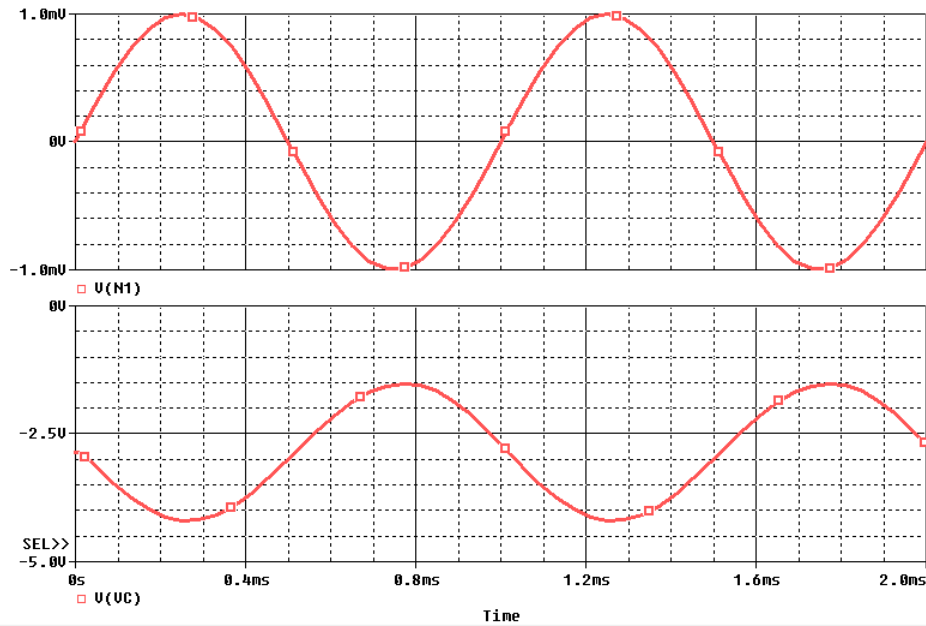
8. Run the netlist and perform an operating point analysis. The node voltages are

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( N1)	0.0000	( N2)	-.5957	( N3)	-2.1924	( VC)	-2.8567
( VDD)	10.0000	( VSS)	-10.0000				

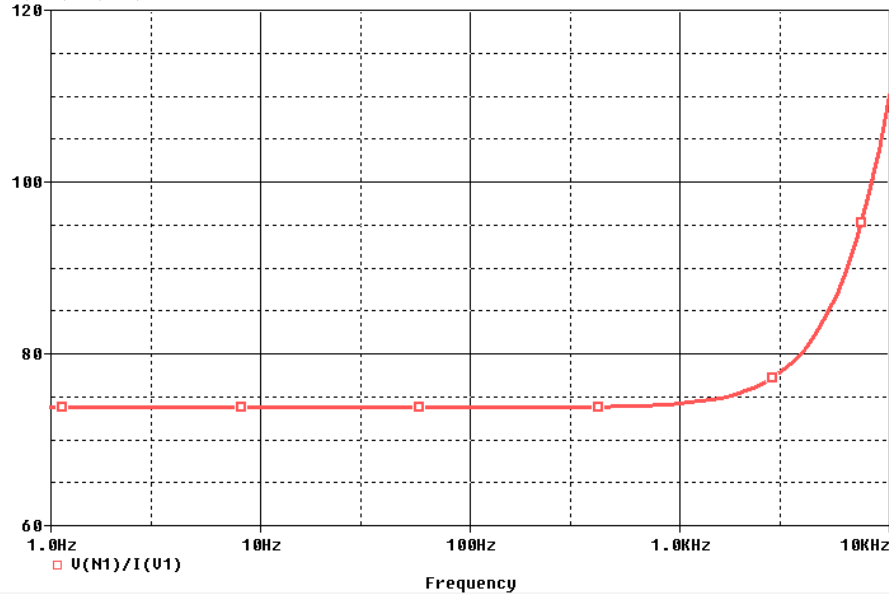
9. The dc currents of the transistors are

NAME	Q1	Q2
MODEL	QPNP	QNPN
IB	-1.42E-06	1.44E-05
IC	-1.44E-05	9.63E-04

10. Run the netlist and perform a transient analysis. Plot the voltages at the input V(N1) and output node V(VC) and find the gain.



11. The gain from this simulation is 1335 V/V.
12. Perform an AC simulation and calculate the input impedance by plotting the expression  $V(N1)/I(V1)$ .



13. The input impedance is 74  $\Omega$ .

**Netlist:**

Copy the netlist given below and paste it into a text file and save it with \*.cir extension.

```

*****Problem: P12_39 *****
***** Main circuit begins here*****
R1      N2 VDD  500k TC=0,0
R2      VC N2  100k TC=0,0
I1      VC VSS DC 1mAdc
C1      N1 N2  1  TC=0,0
V1      N1 0 AC 10m
+SIN 0 1m 1k 0 0 0
V2      VDD 0 10Vdc
V3      0 VSS 10Vdc
Q1      N3 N2 0 QPNP
Q2      0 N3 VC QNPN
***** Main circuit ends here*****
***** Q2N3906 model begins here *****
.model QPNP PNP(Is=1.41f Xti=3 Eg=1.11 Vaf=100 Bf=10 Ne=1.5 Ise=0
+           Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p
+           Mjc=.5776 Vjc=.7 Fc=.5 Cje=8.063p Mje=.3677 Vje=.7 Tr=33.42n
+           Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)
***** Q2N3906 model ends here *****

***** Q2N3904 model begins here *****
.model QNPN NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=100 Bf=100 Ne=1.259
+           Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+           Cjc=3.638p Mjc=.3085 Vjc=.7 Fc=.5 Cje=4.493p Mje=.2593 Vje=.7
+           Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
***** Q2N3904 model ends here *****

***** Analysis begins here*****
.OP
*.TRAN 10uS 2mS
*.AC DEC 20 1 10K
.PROBE
.END
***** Analysis ends here*****

```