Microelectronic Circuits International 8th Edition

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Spice Problems Solutions
Chapter 9

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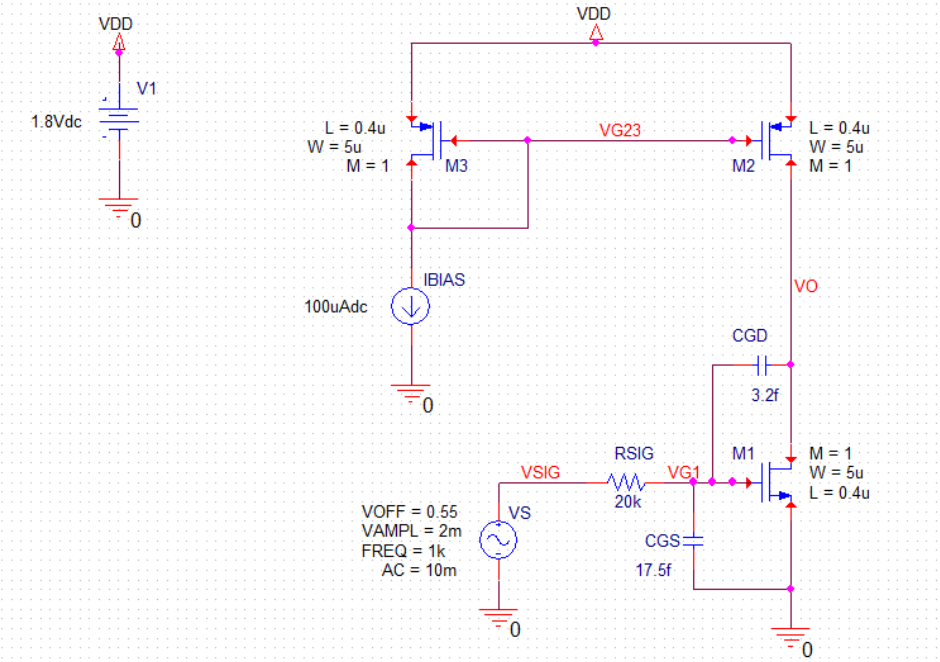
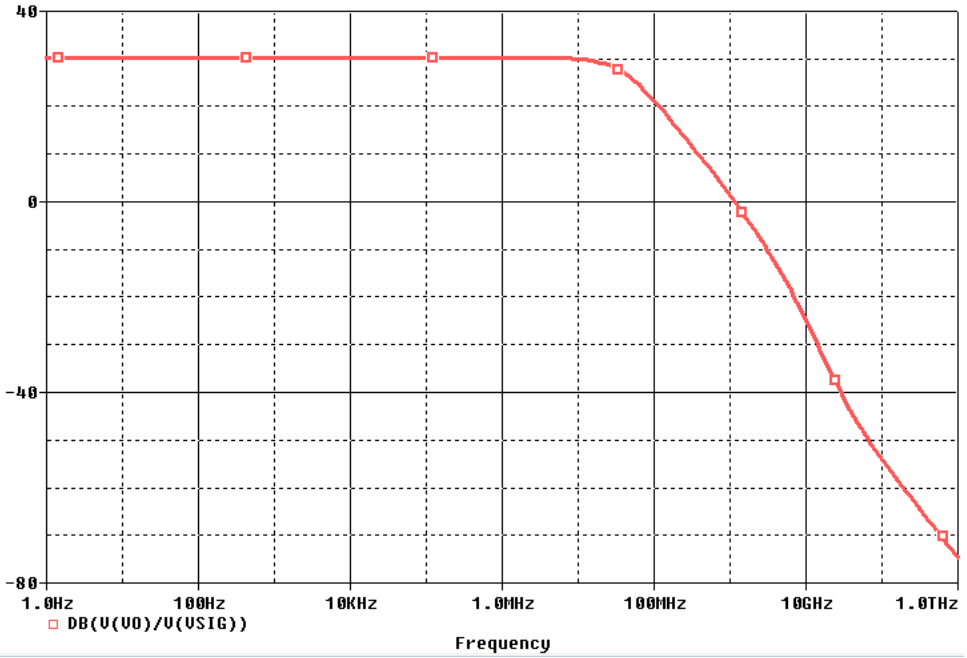
Problem: 9.27

1. The schematic for this problem is shown below.



2. Note that external capacitances are added to match the transistor capacitances given in the problem. The parasitic capacitances from the device are CGS=12.5fF and CGD=1.8fF.

3. Run the netlist and perform AC analysis and plot DB(V(VO)/V(VSIG)).



4. The two frequencies are f_H=38 MHz and f_Z=40 GHz.

Netlist:

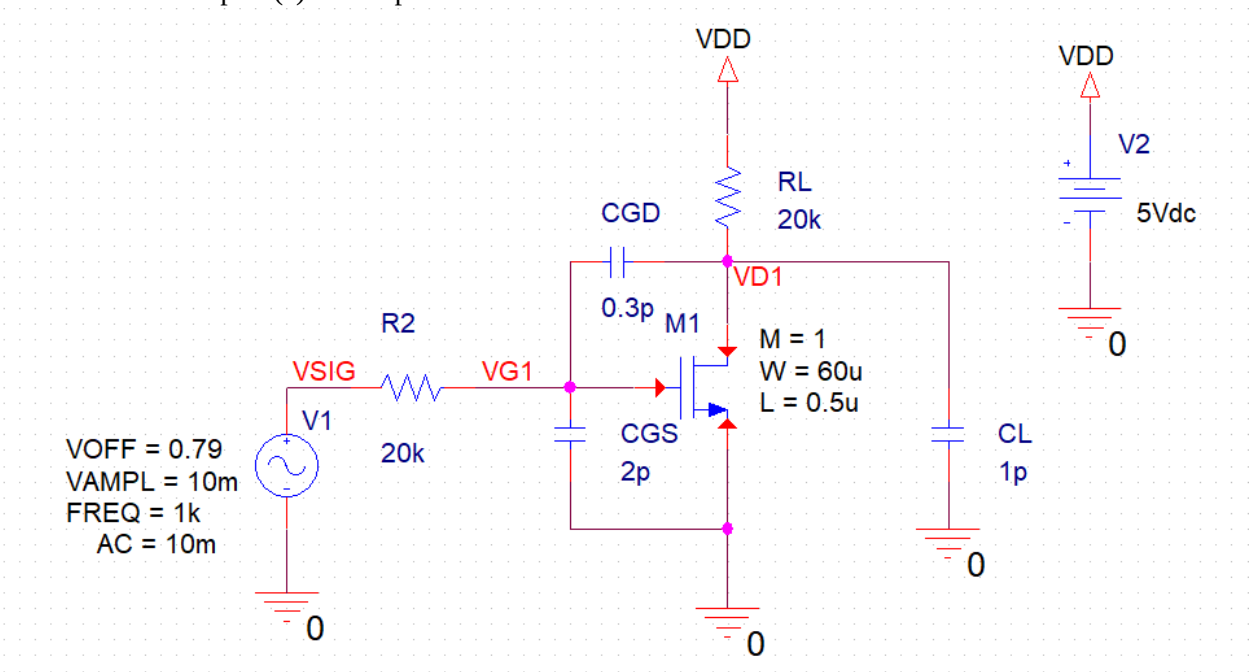
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P10_22               ***************
******* Main circuit begins here**************
IBIAS          VG23 0 DC 100uAdc
RSIG          VSIG VG1  20k TC=0,0
VS          VSIG 0  AC 10m
+SIN 0.58 2m 1k 0 0 0
V1          VDD 0 1.8Vdc
M1          VO VG1 0 0 NMOS0P18
+ L=0.4u
+ W=5u
+ M=1
M2          VO VG23 VDD VDD PMOS0P18
+ L=0.4u
+ W=5u
+ M=1
M3          VG23 VG23 VDD VDD PMOS0P18
+ L=0.4u
+ W=5u
+ M=1
CGS          0 VG1  17.5f
CGD          VO VG1  3.2f
******* Main circuit ends here***************
***************** PMOS model begins here ******************************
.model PMOS0P18        PMOS(Level=1 VTO=-0.4 GAMMA=0.3 PHI=0.8
+               LD=0 WD=0 UO=118 LAMBDA=0.2 TOX=4.08E-9 PB=0.9 CJ=1E-3
+               CJSW=2.04E-10 MJ=0.45 MJSW=0.29 CGDO=3.43E-10 JS=4.0E-7 CGBO=3.5E-10
+               CGSO=3.43E-10)
***************** PMOS model ends here ***************************************
***************** NMOS model begins here ******************************
.model NMOS0P18        NMOS(Level=1 VTO=0.4 GAMMA=0.3 PHI=0.84
+               LD=0 WD=0 UO=473 LAMBDA=0.2 TOX=4.08E-9 PB=0.9 CJ=1.6E-3
+               CJSW=2.04E-10 MJ=0.5 MJSW=0.11 CGDO=3.67E-10 JS=8.38E-6 CGBO=3.8E-10
+               CGSO=3.67E-10)
***************** NMOS model ends here ***************************************


******** Analysis begins here****************
.OP
.AC  DEC   20  1 1T
.PROBE
.END
******** Analysis ends here****************
```

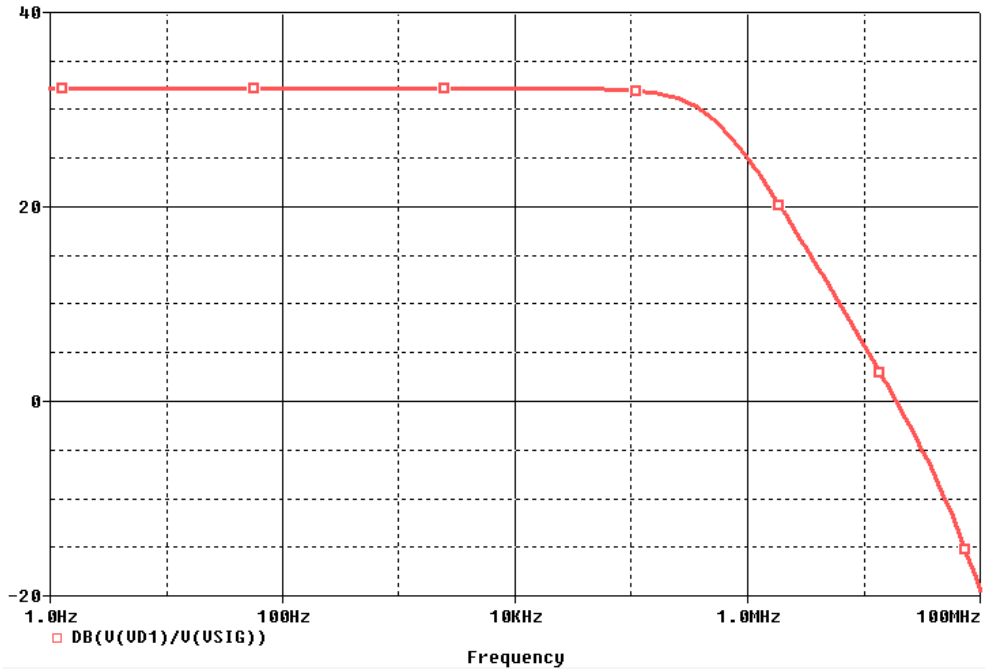
Problem: 9.59

1. The schematic for part (a) of this problem is shown below.

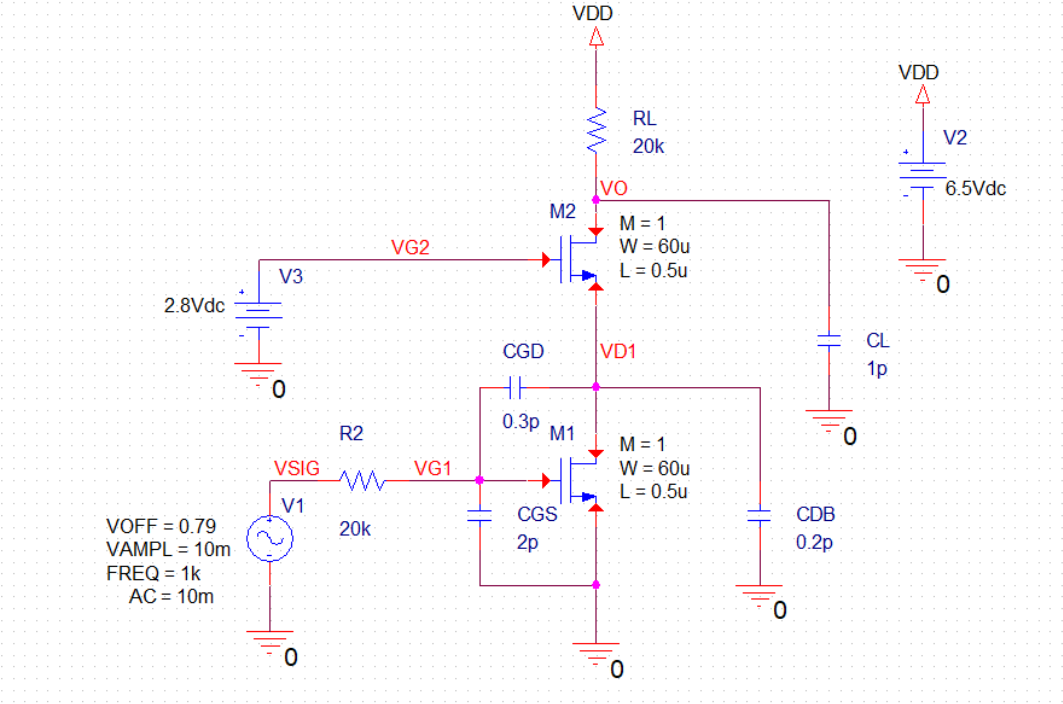


2. For the transistor models used, k'_n=167 µA/V^2. So, the W/L is 120 to get the specified g_m.

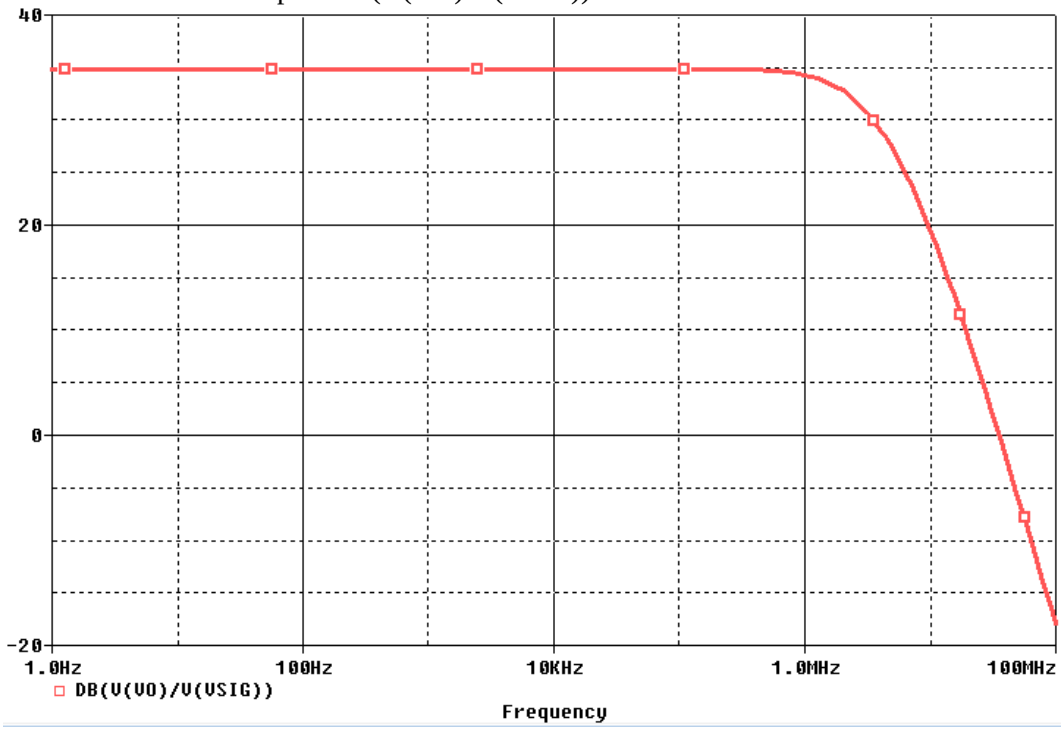
3. Run AC simulation and plot DB(V(VD1)/V(VSIG)). The gain is 40.55 V/V. The unity-gain frequency is at 19.27 MHz.



4. The schematic for part (b) of this problem is shown below.



5. Run an AC simulation and plot DB(V(VO)/V(VSIG)).



6. The unity gain frequency is at 35.5 MHz. This is significantly lower than the gain-bandwidth product because the AC response is decreasing faster than -20 dB/decade between 10 and 100 MHz.

Netlist:

For part (a), copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P10_57 (a) ***************
******* Main circuit begins here**************
V1          VSIG 0  AC 10m
+SIN 0.79 10m 1k 0 0 0
RL          VD1 VDD  20k TC=0,0
R2          VG1 VSIG  20k TC=0,0
V2          VDD 0 5Vdc
M1          VD1 VG1 0 0 NMOS0P5
+ L=0.5u
+ W=60u
+ M=1
CGS          0 VG1  2p  TC=0,0
CGD          VD1 VG1  0.3p  TC=0,0
CL          0 VD1  1p  TC=0,0
******* Main circuit ends here***************

***************** NMOS model begins here *****************************
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+               LD=0 WD=0 UO=460 LAMBDA=0.33 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
***************** NMOS model ends here ****************************************

******** Analysis begins here****************
.OP
.AC  DEC   20  1 100MEG
.PROBE
.END
******** Analysis ends here****************
```

For part (b), copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P10_57 (b) ***************
******* Main circuit begins here**************
V2          VDD 0 6.5Vdc
RL          VO VDD  20k TC=0,0
M2          VO VG2 VD1 0 NMOS0P5
+ L=0.5u
+ W=60u
+ M=1
V3          VG2 0 2.8Vdc
V1          VSIG 0  AC 10m
+SIN 0.79 10m 1k 0 0 0
R2          VG1 VSIG  20k TC=0,0
CGS          0 VG1  2p  TC=0,0
CDB          0 VD1  0.2p  TC=0,0
CGD          VD1 VG1  0.3p  TC=0,0
M1          VD1 VG1 0 0 NMOS0P5
+ L=0.5u
+ W=60u
+ M=1
CL          0 VO  1p  TC=0,0
******* Main circuit ends here***************

***************** NMOS model begins here *****************************
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+               LD=0 WD=0 UO=460 LAMBDA=0.33 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
***************** NMOS model ends here ****************************************

******** Analysis begins here****************
.OP
.AC  DEC   20  1 100MEG
.PROBE
```

```
.END
******** Analysis ends here****************
```