Summary Tables Supplement

Table 1.1 The Four Amplifier Types

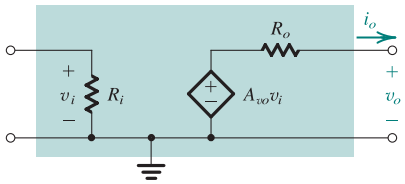
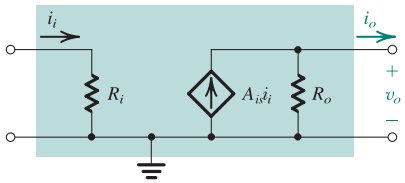
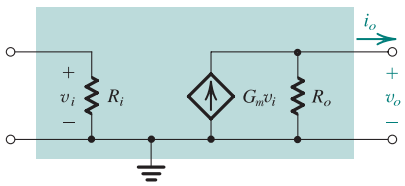
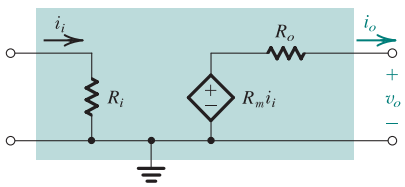
Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} \equiv \left.\frac{v_o}{v_i}\right\|_{i_o=0}$ (V/V)	$R_i = \infty$ $R_o = 0$
Current Amplifier		Short-Circuit Current Gain $A_{is} \equiv \left.\frac{i_o}{i_i}\right\|_{v_o=0}$ (A/A)	$R_i = 0$ $R_o = \infty$
Transconductance Amplifier		Short-Circuit Transconductance $G_m \equiv \left.\frac{i_o}{v_i}\right\|_{v_o=0}$ (A/V)	$R_i = \infty$ $R_o = \infty$
Transresistance Amplifier		Open-Circuit Transresistance $R_m \equiv \left.\frac{v_o}{i_i}\right\|_{i_o=0}$ (V/A)	$R_i = 0$ $R_o = 0$

Table 1.2 Frequency Response of STC Networks

	Low-Pass (LP)	High-Pass (HP)
Transfer Function $T(s)$	$\dfrac{K}{1+(s/\omega_0)}$	$\dfrac{Ks}{s+\omega_0}$
Transfer Function (for physical frequencies) $T(j\omega)$	$\dfrac{K}{1+j(\omega/\omega_0)}$	$\dfrac{K}{1-j(\omega_0/\omega)}$
Magnitude Response $\lvert T(j\omega)\rvert$	$\dfrac{\lvert K\rvert}{\sqrt{1+(\omega/\omega_0)^2}}$	$\dfrac{\lvert K\rvert}{\sqrt{1+(\omega_0/\omega)^2}}$
Phase Response $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega = 0$ (dc)	K	0
Transmission at $\omega = \infty$	0	K
3-dB Frequency	$\omega_0 = 1/\tau$; $\tau \equiv$ time constant $\tau = CR$ or L/R	
Bode Plots	in Fig. 1.23	in Fig. 1.24

Table 1.3 Summary of Important Semiconductor Equations

Quantity	Relationship	Values of Constants and Parameters (for Intrinsic Si at $T = 300$ K)
Carrier concentration in intrinsic silicon (cm^{-3})	$n_i = BT^{3/2}e^{-E_g/2kT}$	$B = 7.3 \times 10^{15}$ $cm^{-3}K^{-3/2}$ $E_g = 1.12$ eV $k = 8.62 \times 10^{-5}$ eV/K $n_i = 1.5 \times 10^{10}/cm^3$
Diffusion current density (A/cm^2)	$J_p = -qD_p\frac{dp}{dx}$ $J_n = qD_n\frac{dn}{dx}$	$q = 1.60 \times 10^{-19}$ coulomb $D_p = 12$ cm^2/s $D_n = 34$ cm^2/s
Drift current density (A/cm^2)	$J_{\text{drift}} = q(p\mu_p + n\mu_n)E$	$\mu_p = 480$ $cm^2/V \cdot s$ $\mu_n = 1350$ $cm^2/V \cdot s$
Resistivity ($\Omega \cdot$ cm)	$\rho = 1/[q(p\mu_p + n\mu_n)]$	μ_p and μ_n decrease with the increase in doping concentration
Relationship between mobility and diffusivity	$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T$	$V_T = kT/q \simeq 25.9$ mV
Carrier concentration in n-type silicon (cm^{-3})	$n_{n0} \simeq N_D$ $p_{n0} = n_i^2/N_D$	
Carrier concentration in p-type silicon (cm^{-3})	$p_{p0} \simeq N_A$ $n_{p0} = n_i^2/N_A$	
Junction built-in voltage (V)	$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$	
Width of depletion region (cm)	$\frac{x_n}{x_p} = \frac{N_A}{N_D}$ $W = x_n + x_p$ $= \sqrt{\frac{2e_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + V_R)}$	$e_s = 11.7e_0$ $e_0 = 8.854 \times 10^{-14}$ F/cm

Table 1.3 *continued*

Quantity	Relationship	Values of Constants and Parameters (for Intrinsic Si at $T = 300$ K)
Charge stored in depletion layer (coulomb)	$Q_J = q\dfrac{N_A N_D}{N_A + N_D} AW$	
Forward current (A)	$I = I_p + I_n$ $I_p = Aqn_i^2 \dfrac{D_p}{L_p N_D}\left(e^{V/V_T} - 1\right)$ $I_n = Aqn_i^2 \dfrac{D_n}{L_n N_A}\left(e^{V/V_T} - 1\right)$	
Saturation current (A)	$I_S = Aqn_i^2\left(\dfrac{D_p}{L_p N_D} + \dfrac{D_n}{L_n N_A}\right)$	
I–V relationship	$I = I_S\left(e^{V/V_T} - 1\right)$	
Minority-carrier lifetime (s)	$\tau_p = L_p^2/D_p \qquad \tau_n = L_n^2/D_n$	$L_p, L_n = 1\ \mu$m to $100\ \mu$m $\tau_p, \tau_n = 1$ ns to 10^4 ns
Minority-carrier charge storage (coulomb)	$Q_p = \tau_p I_p \qquad Q_n = \tau_n I_n$ $Q = Q_p + Q_n = \tau_T I$	
Depletion capacitance (F)	$C_{j0} = A\sqrt{\left(\dfrac{e_s q}{2}\right)\left(\dfrac{N_A N_D}{N_A + N_D}\right)\dfrac{1}{V_0}}$ $C_j = C_{j0}\Big/\left(1 + \dfrac{V_R}{V_0}\right)^m$	$m = \dfrac{1}{3}$ to $\dfrac{1}{2}$
Diffusion capacitance (F)	$C_d = \left(\dfrac{\tau_T}{V_T}\right)I$	

Table 2.1 Characteristics of the Ideal Op Amp

1. Infinite input impedance
2. Zero output impedance
3. Zero common-mode gain or, equivalently, infinite common-mode rejection
4. Infinite open-loop gain A
5. Infinite bandwidth

Table 3.1 Diode models

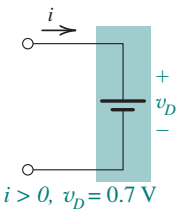
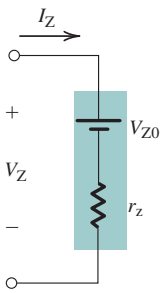
Exact	$i = I_S(e^{v/V_T} - 1), \quad V_T = \frac{kT}{q}$ k = Boltzmann's constant = 8.62×10^{-5} eV/K = 1.38×10^{-23} J/K T = the absolute temperature in Kelvin = 273 + temperature in °C q = the magnitude of electronic charge = 1.60×10^{-19} coulomb $V_2 - V_1 = 2.3\, V_T \log \frac{I_2}{I_1}$
Constant voltage drop model	 $i > 0,\ v_D = 0.7$ V
Reverse bias model	 $V_Z = V_{Z0} + r_z I_Z$
Small-signal model	$r_d = \frac{V_T}{I_D}$

Table 4.1 BJT Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

Table 4.2 Summary of the BJT Current–Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

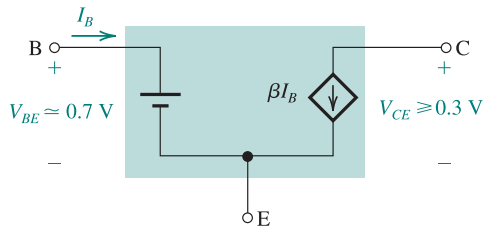
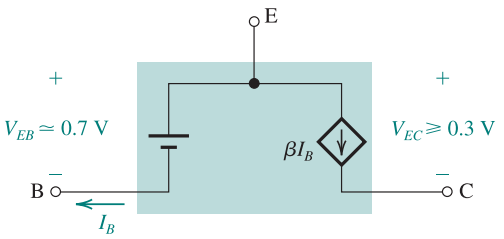
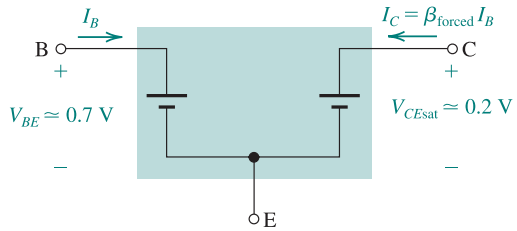
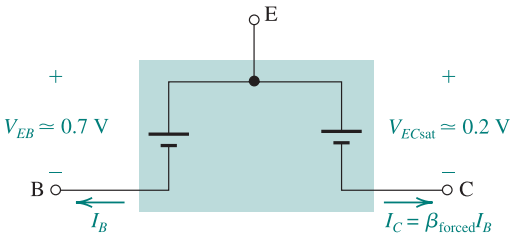
$$i_C = \alpha i_E \qquad i_B = (1-\alpha) i_E = \frac{i_E}{\beta+1}$$

$$i_C = \beta i_B \qquad i_E = (\beta+1) i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

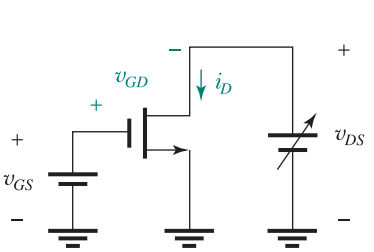
V_T = thermal voltage $= \dfrac{kT}{q} \simeq 25$ mV at room temperature

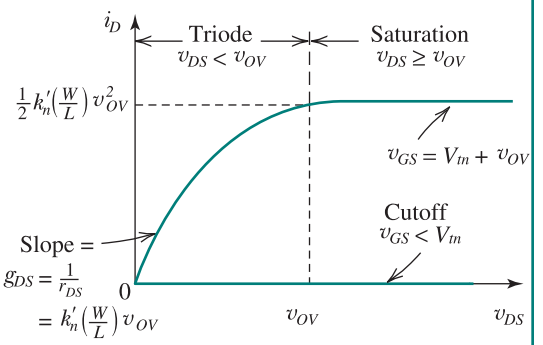
Table 4.3 Simplified Models for the Operation of the BJT in DC Circuits

	npn	*pnp*
Active EBJ: Forward Biased; CBJ: Reverse Biased		
Saturation EBJ: Forward Biased; CBJ: Forward Biased		

$\beta_{\text{forced}} < \beta_{\text{min}}$

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

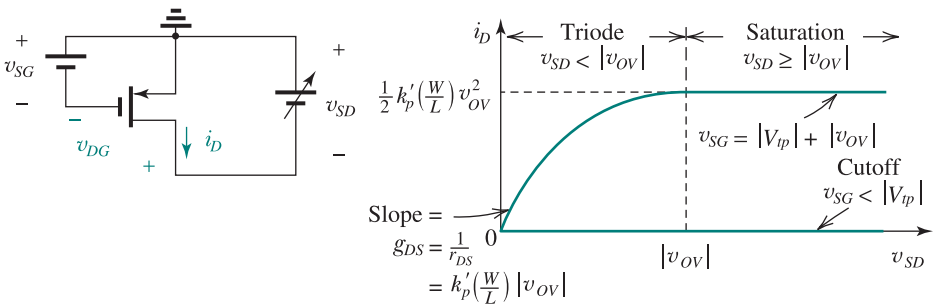
Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor



- $v_{SG} < |V_{tp}|$: no channel; transistor in cutoff; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 6.1 Systematic Procedure for the Analysis of Transistor Amplifier Circuits

1. Eliminate the signal source and determine the dc operating point of the transistor.
2. Calculate the values of the parameters of the small-signal model.
3. Eliminate the dc sources by replacing each dc voltage source by a short circuit and each dc current source by an open circuit.
4. Replace the transistor with one of its small-signal, equivalent-circuit models. Although any of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point is made clearer in Section 7.3.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance).

Table 6.2 Small-Signal Models of the MOSFET

Small-Signal Parameters

NMOS transistors

- **Transconductance:**

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

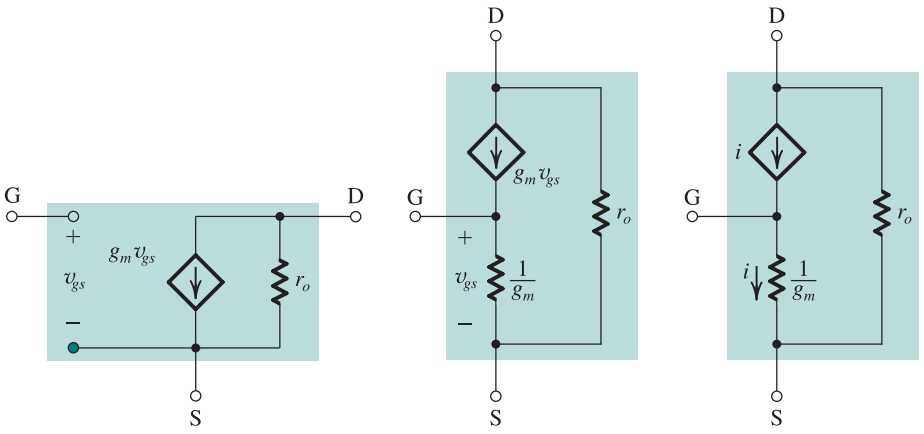
- Output resistance:

$$r_o = V_A / I_D = 1/\lambda I_D$$

PMOS transistors

Same formulas as for NMOS *except* using $|V_{OV}|$, $|V_A|$, $|\lambda|$ and replacing μ_n with μ_p.

Small-Signal, Equivalent-Circuit Models

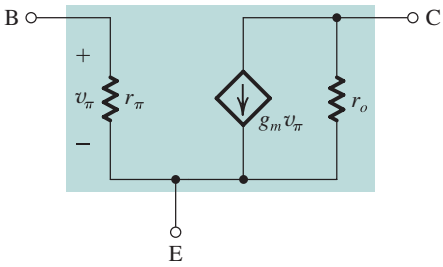


Hybrid-π model T models

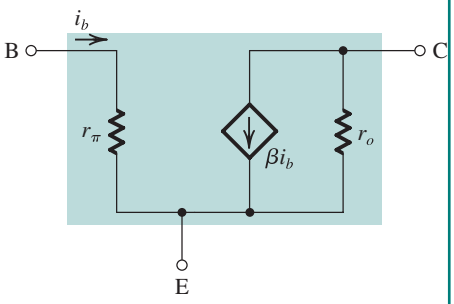
Table 6.3 Small-Signal Models of the BJT

Hybrid-π Model

■ $g_m v_\pi$ Version

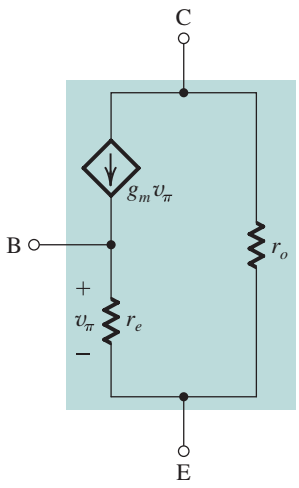


■ βi_b Version

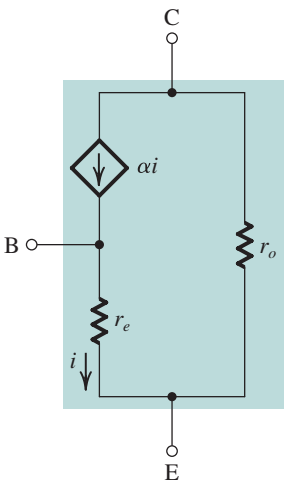


T Model

■ $g_m v_\pi$ Version



■ αi Version



Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\frac{V_T}{I_C} \qquad r_\pi = \frac{V_T}{I_B} = \beta\frac{V_T}{I_C} \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta + 1 = \frac{1}{1-\alpha}$$

Table 6.4 Characteristics of MOSFET Amplifiers[a,b]

Amplifier type	Characteristics				
	R_{in}	A_{vo}	R_o	A_v	G_v
Common source (Fig. 6.36)	∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_s (Fig. 6.38)	∞	$-\dfrac{g_m R_D}{1+g_m R_s}$	R_D	$\dfrac{-g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$	$-\dfrac{g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate (Fig. 6.40)	$\dfrac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\dfrac{R_D \parallel R_L}{R_{\text{sig}} + 1/g_m}$
Source follower (Fig. 6.43)	∞	1	$\dfrac{1}{g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$

[a] For the interpretation of R_{in}, A_{vo}, and R_o, refer to Fig. 6.35(b).
[b] The MOSFET output resistance r_o is not taken into account in these formulas.

Table 6.5 Characteristics of BJT Amplifiers[a,b,c]

	R_{in}	A_{vo}	R_o	A_v	G_v
Common emitter (Fig. 6.37)	$(\beta+1)r_e$	$-g_m R_C$	R_C	$-g_m(R_C \parallel R_L)$ $-\alpha\dfrac{R_C \parallel R_L}{r_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{\text{sig}} + (\beta+1)r_e}$
Common emitter with R_e (Fig. 6.39)	$(\beta+1)(r_e + R_e)$	$-\dfrac{g_m R_C}{1+g_m R_e}$	R_C	$\dfrac{-g_m(R_C \parallel R_L)}{1+g_m R_e}$ $-\alpha\dfrac{R_C \parallel R_L}{r_e + R_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{\text{sig}} + (\beta+1)(r_e + R_e)}$
Common base (Fig. 6.41)	r_e	$g_m R_C$	R_C	$g_m(R_C \parallel R_L)$ $\alpha\dfrac{R_C \parallel R_L}{r_e}$	$\alpha\dfrac{R_C \parallel R_L}{R_{\text{sig}} + r_e}$
Emitter follower (Fig. 6.44)	$(\beta+1)(r_e + R_L)$	1	r_e	$\dfrac{R_L}{R_L + r_e}$	$\dfrac{R_L}{R_L + r_e + R_{\text{sig}}/(\beta+1)}$ $G_{vo} = 1$ $R_{\text{out}} = r_e + \dfrac{R_{\text{sig}}}{\beta+1}$

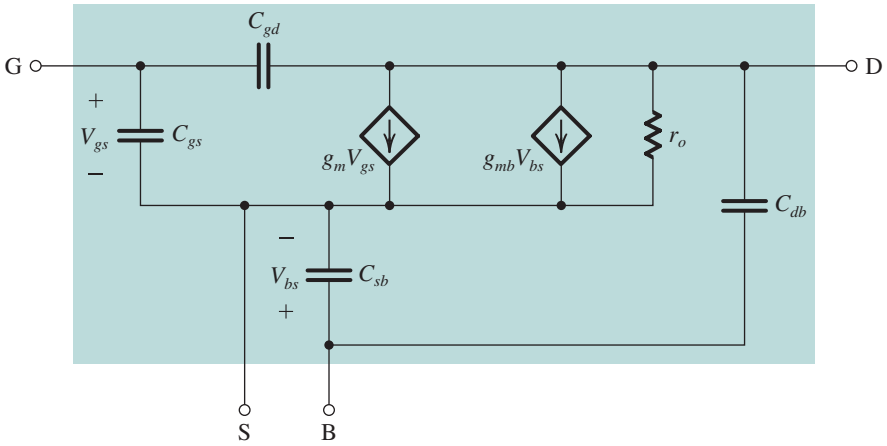
[a] For the interpretation of R_m, A_{vo}, and R_o refer to Fig. 6.35.
[b] The BJT output resistance r_o is not taken into account in these formulas.
[c] Setting $\beta = \infty$ ($\alpha = 1$) and replacing r_e with $1/g_m$, R_C with R_D, and R_e with R_s results in the corresponding formulas for MOSFET amplifiers (Table 6.4).

Table 7.1 Gain Distribution in the MOS Cascode Amplifier for Various Values of R_L

Case	R_L	R_{in2}	R_{d1}	A_{v1}	A_{v2}	A_v
1	∞	∞	r_o	$-g_m r_o$	$g_m r_o$	$-(g_m r_o)^2$
2	$(g_m r_o) r_o$	r_o	$r_o/2$	$-\frac{1}{2}(g_m r_o)$	$g_m r_o$	$-\frac{1}{2}(g_m r_o)^2$
3	r_o	$\frac{2}{g_m}$	$\frac{2}{g_m}$	-2	$\frac{1}{2}(g_m r_o)$	$-(g_m r_o)$
4	$0.2 r_0$	$\frac{1.2}{g_m}$	$\frac{1.2}{g_m}$	-1.2	$0.17(g_m r_o)$	$-0.2(g_m r_o)$

Table 9.1 The MOSFET High-Frequency Model

Model



Model Parameters

$$g_m = \mu_n C_{ox} \frac{W}{L} |V_{OV}| = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{|V_{OV}|}$$

$$g_{mb} = \chi g_m, \quad \chi = 0.1 \text{ to } 0.2$$

$$r_o = |V_A|/I_D$$

$$C_{gs} = \frac{2}{3} WLC_{ox} + WL_{ov}C_{ox}$$

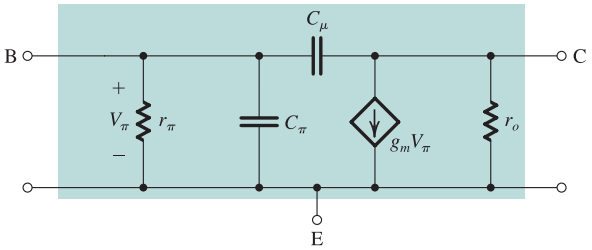
$$C_{gd} = WL_{ov}C_{ox}$$

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{|V_{SB}|}{V_0}}}$$

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{|V_{DB}|}{V_0}}}$$

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Table 9.2 The BJT High-Frequency Model



$g_m = I_C/V_T$ $\quad r_o = |V_A|/I_C$ $\quad r_\pi = \beta_0/g_m$

$C_\pi + C_\mu = \dfrac{g_m}{2\pi f_T}$ $\quad C_\pi = C_{de} + C_{je}$ $\quad C_{de} = \tau_F g_m$ $\quad C_{je} \simeq 2C_{je0}$

$C_\mu = C_{jc0} \Big/ \left(1 + \dfrac{|V_{CB}|}{V_{0c}}\right)^m$ $\quad m = 0.3\text{–}0.5$

Table 10.1 Summary of the Parameters and Formulas for the Ideal Feedback-Amplifier Structure of Fig. 10.1

- Open-loop gain $\equiv A$
- Feedback factor $\equiv \beta$
- Loop gain $\equiv A\beta$ (positive number)
- Amount of feedback $\equiv 1 + A\beta$
- Closed-loop gain $\equiv A_f = \dfrac{x_o}{x_s} = \dfrac{A}{1+A\beta}$
- Feedback signal $\equiv x_f = \dfrac{A\beta}{1+A\beta} x_s$
- Input signal to basic amplifier $\equiv x_i = \dfrac{1}{1+A\beta} x_s$
- $A_f|_{\text{ideal}} = \dfrac{1}{\beta}$
- Closed-loop gain as a function of the ideal value $\dfrac{1}{\beta}$: $A_f = \left(\dfrac{1}{\beta}\right) \dfrac{1}{1+1/A\beta}$
- For $A = \infty$, $x_i = 0$, $x_f = x_s$, $x_o = \dfrac{1}{\beta} x_s$, $A_f = A_f|_{\text{ideal}} = \dfrac{1}{\beta}$
- For large loop gain, $A\beta \gg 1$,

  $A_f \simeq \dfrac{1}{\beta}$ $\quad x_f \simeq x_s$ $\quad x_i \simeq 0$

Table 10.2 Summary of Relationships for the Four Feedback-Amplifier Topologies

Feedback Amplifier	Feedback Topology	x_i	x_o	x_f	x_s	A	β	A_f	Source Form	Loading of Feedback Network Is Obtained: At Input	Loading of Feedback Network Is Obtained: At Output	To Find β, Apply to Port 2 of Feedback Network	R_{if}	R_{of}	Refer to Figs.
Voltage	Series–Shunt	V_i	V_o	V_f	V_s	$\frac{V_o}{V_i}$	$\frac{V_f}{V_o}$	$\frac{V_o}{V_s}$	Thévenin	By short-circuiting port 2 of feedback network	By open-circuiting port 1 of feedback network	a voltage, and find the open-circuit voltage at port 1	$R_i(1+A\beta)$	$\frac{R_o}{1+A\beta}$	11.14 11.16
Current	Shunt–Series	I_i	I_o	I_f	I_s	$\frac{I_o}{I_i}$	$\frac{I_f}{I_o}$	$\frac{I_o}{I_s}$	Norton	By open-circuiting port 2 of feedback network	By short-circuiting port 1 of feedback network	a current, and find the short-circuit current at port 1	$\frac{R_i}{1+A\beta}$	$R_o(1+A\beta)$	11.28 11.29
Transconductance	Series–Series	V_i	I_o	V_f	V_s	$\frac{I_o}{V_i}$	$\frac{V_f}{I_o}$	$\frac{I_o}{V_s}$	Thévenin	By open-circuiting port 2 of feedback network	By open-circuiting port 1 of feedback network	a current, and find the open-circuit voltage at port 1	$R_i(1+A\beta)$	$R_o(1+A\beta)$	11.21 11.22
Transresistance	Shunt–Shunt	I_i	V_o	I_f	I_s	$\frac{V_o}{I_i}$	$\frac{I_f}{V_o}$	$\frac{V_o}{I_s}$	Norton	By short-circuiting port 2 of feedback network	By short-circuiting port 1 of feedback network	a voltage, and find the short-circuit current at port 1	$\frac{R_i}{1+A\beta}$	$\frac{R_o}{1+A\beta}$	11.25 11.26

Table 14.1 Important Parameters of the VTC of the Logic Inverter (Refer to Fig. 14.13)

V_{OL}:	Output low level
V_{OH}:	Output high level
V_{IL}:	Maximum value of input interpreted by the inverter as a logic 0
V_{IH}:	Minimum value of input interpreted by the inverter as a logic 1
NM_L:	Noise margin for low input $= V_{IL} - V_{OL}$
NM_H:	Noise margin for high input $= V_{OH} - V_{IH}$

Table 14.2 Summary of Important Static Characteristics of the CMOS Logic Inverter

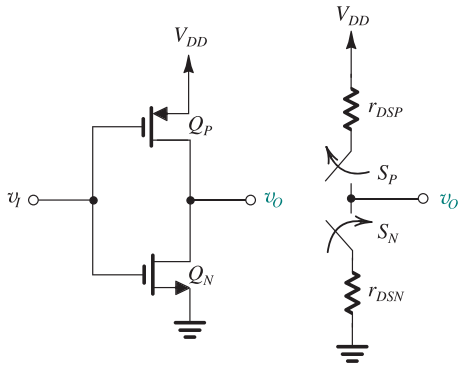
Inverter Output Resistance

- When v_O is low (current sinking):

$$r_{DSN} = 1\Big/\left[k_n'\left(\frac{W}{L}\right)_n(V_{DD} - V_{tn})\right]$$

- When v_O is high (current sourcing):

$$r_{DSP} = 1\Big/\left[k_p'\left(\frac{W}{L}\right)_p(V_{DD} - |V_{tp}|)\right]$$



Inverter VTC and Noise Margins

$$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{1 + r} \quad \text{where} \quad r = \sqrt{\frac{k_p'(W/L)_p}{k_n'(W/L)_n}}$$

For matched devices, that is, $\mu_n\left(\frac{W}{L}\right)_n = \mu_p\left(\frac{W}{L}\right)_p$, and $V_{tn} = -V_{tp} = V_t$

$r = 1$

$V_M = V_{DD}/2$

$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$

$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$

$NM_H = NM_L = \frac{1}{8}(3V_{DD} + 2V_t)$

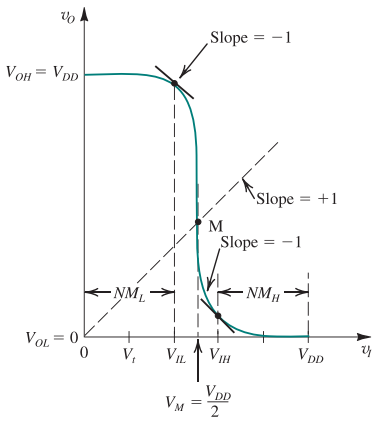


Table 15.1 Implications of Device and Voltage Scaling

	Parameter	Relationship	Scaling Factor
1	W, L, t_{ox}		$1/S$
2	V_{DD}, V_t		$1/S$
3	Area/Device	WL	$1/S^2$
4	C_{ox}	ϵ_{ox}/t_{ox}	S
5	k_n', k_p'	$\mu_n C_{ox}, \mu_p C_{ox}$	S
6	C_{gate}	WLC_{ox}	$1/S$
7	t_P (intrinsic)	$\alpha C/k' V_{DD}$	$1/S$
8	Energy/Switching cycle (intrinsic)	CV_{DD}^2	$1/S^3$
9	P_{dyn}	$f_{\max} CV_{DD}^2 = \dfrac{CV_{DD}^2}{2t_P}$	$1/S^2$
10	Power density	P_{dyn}/Device area	1

Table 15.2 Summary of Important Speed and Power Characteristics of the CMOS Logic Inverter

Propagation Delay

Using average currents (Fig. 15.4):

$$t_{PHL} \simeq \frac{\alpha_n C}{k_n'(W/L)_n V_{DD}} \text{ where } \alpha_n = \frac{2}{\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2}$$

$$t_{PLH} \simeq \frac{\alpha_p C}{k_p'(W/L)_p V_{DD}} \text{ where } \alpha_p = \frac{2}{\frac{7}{4} - \frac{3|V_{tp}|}{V_{DD}} + \left(\frac{|V_{tp}|}{V_{DD}}\right)^2}$$

Using equivalent resistances (Fig. 15.5):

$$t_{PHL} = 0.69 R_N C \text{ where } R_N = \frac{R_{eff,N}(W_{eff}/L_{eff})}{(W_n/L_n)}$$

$$t_{PLH} = 0.69 R_P C \text{ where } R_P = \frac{R_{eff,P}(W_{eff}/L_{eff})}{(W_p/L_p)}$$

For a ramp-input signal, $t_{PHL} \simeq R_N C$ and $t_{PLH} \simeq R_P C$.

Power Dissipation

$$P_{dyn} = fCV_{DD}^2$$

$$PDP = P_D \times t_P$$

$$EDP = PDP \times t_P$$

Table G.3 Comparison of MOSFET and the BJT

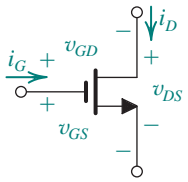
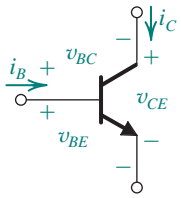
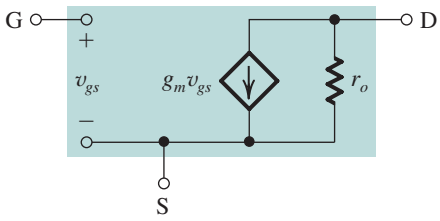
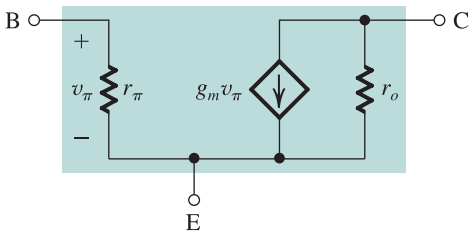
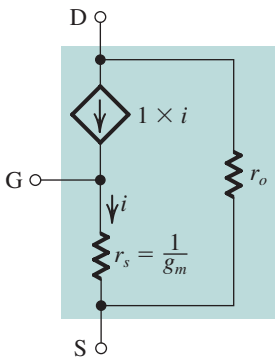
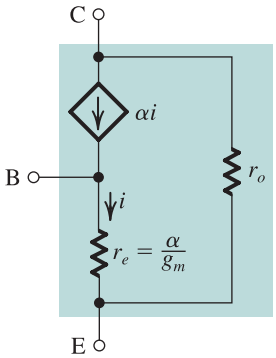
	NMOS	*npn*
Circuit Symbol		
To Operate in the Active Mode, Two Conditions Have to Be Satisfied	(1) *Induce a channel*: $v_{GS} \geq V_t$, $V_t = 0.3$–$0.5\,\text{V}$ Let $v_{GS} = V_t + v_{OV}$ (2) *Pinch-off channel at drain*: $v_{GD} < V_t$ or equivalently, $v_{DS} \geq V_{OV}$, $V_{OV} = 0.1$–$0.3\,\text{V}$	(1) *Forward-bias EBJ:* $v_{BE} \geq V_{BE\text{on}}$, $V_{BE\text{on}} \simeq 0.5\,\text{V}$ (2) *Reverse-bias CBJ:* $v_{BC} < V_{BC\text{on}}$, $V_{BC\text{on}} \simeq 0.4\,\text{V}$ or equivalently, $v_{CE} \geq 0.3\,\text{V}$
Current–Voltage Characteristics in the Active Region	$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2\left(1+\frac{v_{DS}}{V_A}\right)$ $= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2\left(1+\frac{v_{DS}}{V_A}\right)$ $i_G = 0$	$i_C = I_S e^{v_{BE}/V_T}\left(1+\frac{v_{CE}}{V_A}\right)$ $i_B = i_C/\beta$
Low-Frequency, Hybrid-π Model		
Low-Frequency T Model		

Table G.3 *continued*

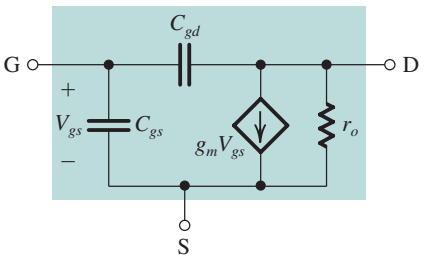
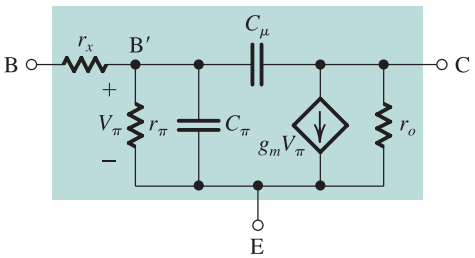
	NMOS	*npn*
Transconductance g_m	$g_m = I_D/(V_{OV}/2)$ $g_m = (\mu_n C_{ox})\left(\frac{W}{L}\right)V_{OV}$ $g_m = \sqrt{2(\mu_n C_{ox})\left(\frac{W}{L}\right)I_D}$	$g_m = I_C/V_T$
Output Resistance r_o	$r_o = V_A/I_D = \frac{V_A' L}{I_D}$	$r_o = V_A/I_C$
Intrinsic Gain $A_0 \equiv g_m r_o$	$A_0 = V_A/(V_{OV}/2)$ $A_0 = \frac{2V_A' L}{V_{OV}}$ $A_0 = \frac{V_A'\sqrt{2\mu_n C_{ox} WL}}{\sqrt{I_D}}$	$A_0 = V_A/V_T$
Input Resistance with Source (Emitter) Grounded	∞	$r_\pi = \beta/g_m$
High-Frequency Model		
Capacitances	$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$ $C_{gd} = WL_{ov}C_{ox}$	$C_\pi = C_{de} + C_{je}$ $C_{de} = \tau_F g_m$ $C_{je} \simeq 2C_{je0}$ $C_\mu = C_{\mu 0}\Big/\left[1 + \frac{V_{CB}}{V_{C0}}\right]^m$
Transition Frequency f_T	$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$ For $C_{gs} \gg C_{gd}$ and $C_{gs} \simeq \frac{2}{3}WLC_{ox}$, $f_T \simeq \frac{1.5\mu_n V_{OV}}{2\pi L^2}$	$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$ For $C_\pi \gg C_\mu$ and $C_\pi \simeq C_{de}$, $f_T \simeq \frac{2\mu_n V_T}{2\pi W_B^2}$
Design Parameters	I_D, V_{OV}, L, $\frac{W}{L}$	I_C, V_{BE}, A_E (or I_S)
Good Analog Switch?	Yes, because the device is symmetrical and thus the i_D–v_{DS} characteristics pass directly through the origin.	No, because the device is asymmetrical with an offset voltage V_{CEoff}.

Table J.1 Standard Resistance Values

	1% Resistor Values (kΩ)			
5% Resistor Values (kΩ)	100–174	178–309	316–549	562–976
10	100	178	316	562
11	102	182	324	576
12	105	187	332	590
13	107	191	340	604
15	110	196	348	619
16	113	200	357	634
18	115	205	365	649
20	118	210	374	665
22	121	215	383	681
24	124	221	392	698
27	127	226	402	715
30	130	232	412	732
33	133	237	422	750
36	137	243	432	768
39	140	249	442	787
43	143	255	453	806
47	147	261	464	825
51	150	267	475	845
56	154	274	487	866
62	158	280	499	887
68	162	287	511	909
75	165	294	523	931
82	169	301	536	953
91	174	309	549	976

Table J.2 SI Unit Prefixes

Name	Symbol	Factor
femto	f	$\times 10^{-15}$
pico	p	$\times 10^{-12}$
nano	n	$\times 10^{-9}$
micro	μ	$\times 10^{-6}$
milli	m	$\times 10^{-3}$
kilo	k	$\times 10^{3}$
mega	M	$\times 10^{6}$
giga	G	$\times 10^{9}$
tera	T	$\times 10^{12}$
peta	P	$\times 10^{15}$

Table J.3 Meter Conversion Factors

$1\,\mu\text{m} = 10^{-4}\ \text{cm} = 10^{-6}\ \text{m}$

$1\ \text{m} = 10^{2}\ \text{cm} = 10^{6}\ \mu\text{m} = 10^{9}\ \text{nm}$

$0.1\,\mu\text{m} = 100\ \text{nm}$

$1\ \text{Å} = 10^{-8}\ \text{cm} = 10^{-10}\ \text{m}$

Table K.1 Typical Values of CMOS Device Parameters

	0.8 μm		0.5 μm		0.25 μm		0.18 μm		0.13 μm		65 nm		28 nm	
Parameter	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
t_{ox} (nm)	15	15	9	9	6	6	4	4	2.7	2.7	1.4	1.4	1.4	1.4
C_{ox} (fF/μm^2)	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6	12.8	12.8	25	25	34	34
μ (cm^2/V·s)	550	250	500	180	460	160	450	100	400	100	216	40	220	200
μC_{ox}(μA/V^2)	127	58	190	68	267	93	387	86	511	128	540	100	750	680
V_{t0} (V)	0.7	–0.7	0.7	–0.8	0.5	–0.6	0.5	–0.5	0.4	–0.4	0.35	–0.35	0.3	–0.3
V_{DD} (V)	5	5	3.3	3.3	2.5	2.5	1.8	1.8	1.3	1.3	1.0	1.0	0.9	0.9
$\lvert V_A' \rvert$ (V/μm)	25	20	20	10	5	6	5	6	5	6	3	3	1.5	1.5
C_{ov} (fF/μm)	0.2	0.2	0.4	0.4	0.3	0.3	0.37	0.33	0.36	0.33	0.33	0.31	0.4	0.4

Table K.2 Typical Parameter Values for BJTs*

	Standard High-Voltage Process		Advanced Low-Voltage Process	
Parameter	*npn*	Lateral *pnp*	*npn*	Lateral *pnp*
A_E (μm^2)	500	900	2	2
I_S (A)	5×10^{-15}	2×10^{-15}	6×10^{-18}	6×10^{-18}
β_0 (A/A)	200	50	100	50
V_A (V)	130	50	35	30
V_{CEO} (V)	50	60	8	18
τ_F	0.35 ns	30 ns	10 ps	650 ps
C_{je0}	1 pF	0.3 pF	5 fF	14 fF
$C_{\mu 0}$	0.3 pF	1 pF	5 fF	15 fF
r_x(Ω)	200	300	400	200

*Adapted from Gray et al. (2001); see Appendix I.