x8

EXTRA TOPICS RELATED TO

Bipolar Digital Integrated Circuits

This supplement contains material removed from previous editions of the textbook. These topics continue to be relevant and for this reason will be of great value to many instructors and students.

The topics presented here relate to several families of digital logic circuits that use bipolar transistors rather than today's more conventional CMOS technology. The material builds upon concepts explored in Chapters 16, 17, and 18 of the eighth edition.

x8.1 TRANSISTOR–TRANSISTOR LOGIC (TTL OR T_2L)

From the late 1960s to the late 1980s, transistor–transistor logic (TTL) enjoyed immense popularity. Indeed, the bulk of digital systems applications employing small-scale integration (SSI) and medium-scale integration (MSI) packages were designed using TTL.

We shall begin this section with a study of how TTL evolved from diode–transistor logic (DTL). In this way we shall explain the function of each of the stages of the complete TTL gate circuit. Characteristics of standard TTL gates will be studied in Section x8.2 of this supplment. More advanced forms of TTL that feature improved performance will be discussed in Section x8.3 of the bonus materials.

x8.1.1 Evolution of TTL from DTL

An integrated-circuit form of a DTL gate is shown in Fig. x8.1 with only one input indicated. As a prelude to introducing TTL, we have drawn the input diode as a diode-connected transistor (Q_1), which corresponds to how diodes are made in IC form.

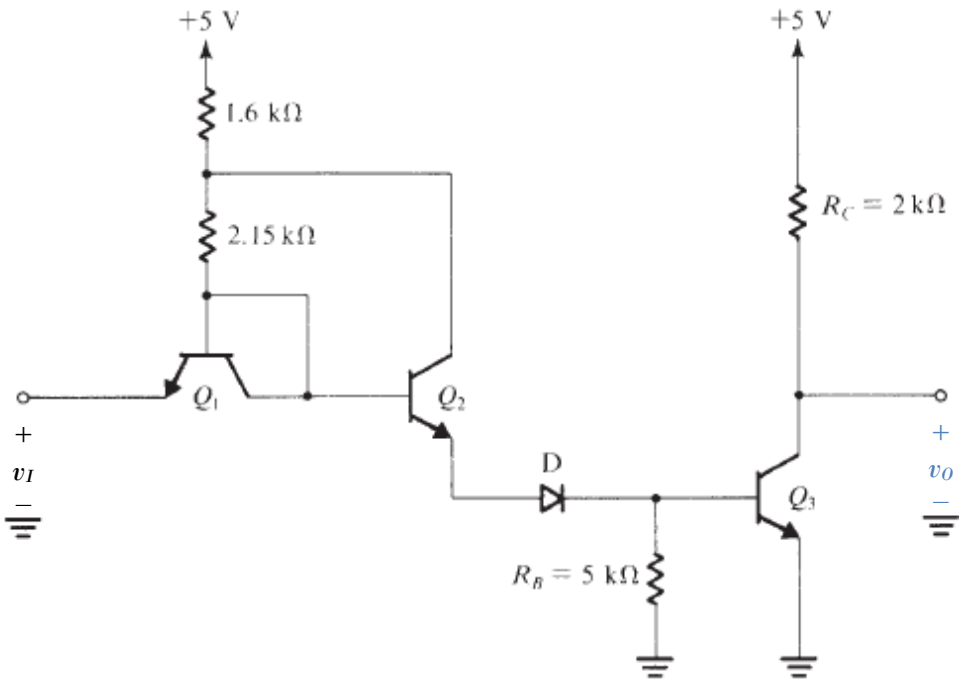

FIGURE x8.1 IC form of the DTL gate with the input diode shown as a diode-connected transistor (Q_1). Only one input terminal is shown.

This circuit differs from a discrete DTL circuit in two important aspects. First, one of the steering diodes is replaced by the base–emitter junction of a transistor (Q_2) that is either cut off (when the input is low) or in the active mode (when the input is high). This is done to reduce the input current and thereby increase the fan-out capability of the gate. A detailed explanation of this point, however, is not relevant to our study of TTL. Second, the resistance R_B is returned to ground rather than to a negative supply, as was done in the earlier discrete circuit. An obvious advantage of this is the elimination of the additional power supply. The disadvantage, however, is that the reverse base current available to remove the excess charge stored in the base of Q_3 is rather small. We shall elaborate on this point below.

EXERCISE

x8.1 Consider the DTL gate circuit shown in Fig. x8.1 and assume that $\beta(Q_2) = \beta(Q_3) = 50$.

(a) When $v_I = 0.2$ V, find the input current.

(b) When $v_I = +5$ V, find the base current of Q_3.

Ans. (a) 1.1 mA; (b) 1.6 mA

x8.1.2 Reasons for the Slow Response of DTL

The DTL gate has relatively good noise margins and reasonably good fan-out capability. Its response, however, is rather slow. There are two reasons for this: first, when the input goes low and Q_2 and D turn off, the charge stored in the base of Q_3 has to leak through R_B to ground. The initial value of the reverse base current that accomplishes this "base discharging" process is approximately 0.7 V/R_B, which is about 0.14 mA. Because this current is quite small in comparison to the forward base current, the time required for the removal of base charge is rather long, which contributes to lengthening the gate delay.

The second reason for the relatively slow response of DTL derives from the nature of the output circuit of the gate, which is simply a common-emitter transistor. Figure x8.2 shows the output transistor of a DTL gate driving a capacitive load C_L. The capacitance C_L represents the input capacitance of another gate and/or the wiring and parasitic capacitances that are inevitably present in any circuit. When Q_3 is turned on, its collector voltage cannot instantaneously fall because of the existence of C_L. Thus Q_3 will not immediately saturate but rather will operate in the active region. The collector of Q_3 will therefore act as a constant-current source and will sink a relatively large current (I_B). This large current will rapidly discharge C_L. We thus see that the common-emitter output stage features a short turn-on time. However, turnoff is another matter.

Consider next the operation of the common-emitter output stage when Q_3 is turned off. The output voltage will not rise immediately to the high level (V_{CC}). Rather, C_L will charge up to V_{CC} through R_C. This is a rather slow process, and it results in lengthening the DTL gate delay (and similarly the RTL gate delay).

Having identified the two reasons for the slow response of DTL, we shall see in the following how these problems are remedied in TTL.

x8.1.3 Input Circuit of the TTL Gate

Figure x8.3 shows a conceptual TTL gate with only one input terminal indicated. The most important feature to note is that the input diode has been replaced by a transistor. One can think of this simply as if the short circuit between base and collector of Q_1 in Fig. x8.1 has been removed.

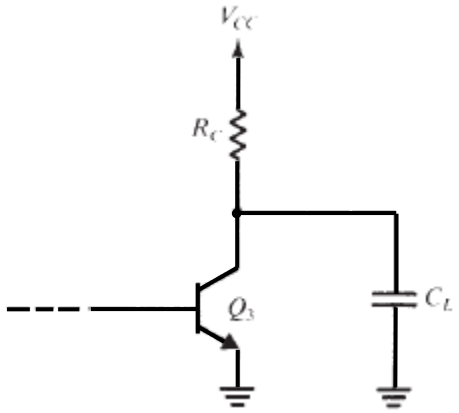

FIGURE x8.2 The output circuit of a DTL gate driving a capacitive load C_L.

To see how the conceptual TTL circuit of Fig. x8.3 works, let the input v_I be high (say, $v_I = V_{CC}$). In this case current will flow from V_{CC} through R, thus forward-biasing the base−collector junction of Q_1. Meanwhile, the base−emitter junction of Q_1 will be reverse-biased. Therefore Q_1 will be operating in the **inverse active mode**—that is, in the active mode but with the roles of emitter and collector interchanged. The voltages and currents will be as indicated in Fig. x8.4, where the current I can be calculated from

$$I = \frac{V_{CC} - 1.4}{R}$$

In actual TTL circuits Q_1 is designed to have a very low reverse β ($\beta_R \simeq 0.02$). Thus the gate input current will be very small, and the base current of Q_3 will be approximately equal to I. This current will be sufficient to drive Q_3 into saturation, and the output voltage will be low (0.1 to 0.2 V).

Next let the gate input voltage be brought down to the logic-0 level (say, $v_I \simeq 0.2$ V). The current I will then be diverted to the emitter of Q_1. The base−emitter junction of Q_1 will become forward-biased, and the base voltage of Q_1 will therefore drop to 0.9 V. Since Q_3 *was* in saturation, its base voltage will remain at +0.7 V pending the removal of the excess charge stored in the base region. Figure x8.5 indicates the various voltage and current values immediately after the input is lowered. We see that Q_1 will be operating in the normal active mode and its collector will carry a large current ($\beta_F I$). This large current

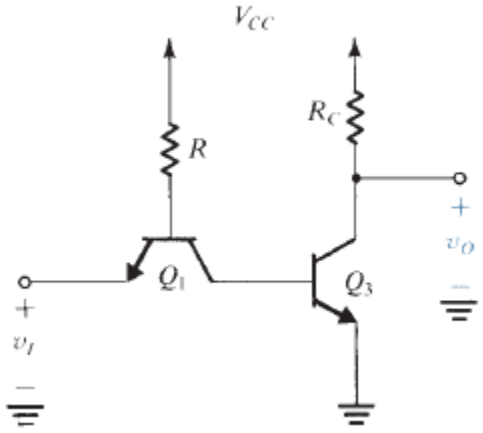

FIGURE x8.3 Conceptual form of TTL gate. Only one input terminal is shown.

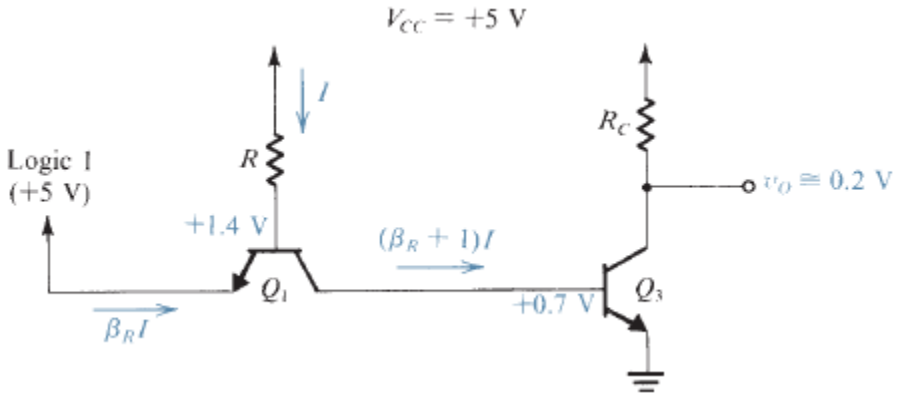

FIGURE x8.4 Analysis of the conceptual TTL gate when the input is high.

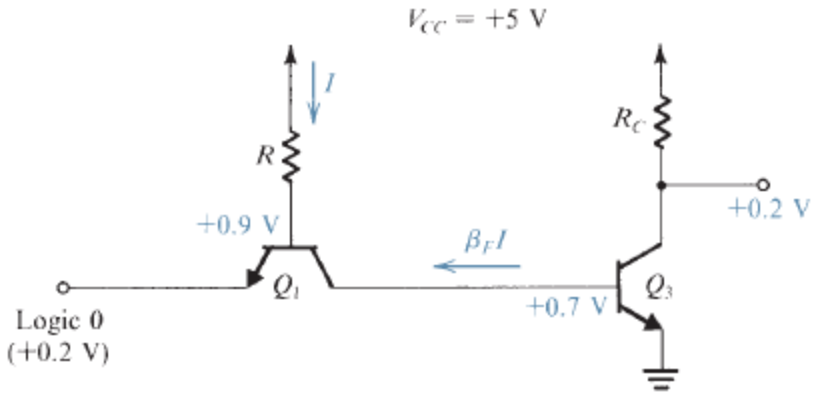

FIGURE x8.5 Voltage and current values in the conceptual TTL circuit immediately after the input voltage is lowered.

rapidly discharges the base of Q_3 and drives it into cutoff. We thus see the action of Q_1 in speeding up the turn-off process.

As Q_3 turns off, the voltage at its base is reduced, and Q_1 enters the saturation mode. Eventually the collector current of Q_1 will become negligibly small, which implies that its V_{CEsat} will be approximately 0.1 V and the base of Q_3 will be at about 0.3 V, which keeps Q_3 in cutoff.

x8.1.4 Output Circuit of the TTL Gate

The above discussion illustrates how one of the two problems that slow down the operation of DTL is solved in TTL. The second problem, the long rise time of the output waveform, is solved by modifying the output stage, as we shall now explain.

First, recall that the common-emitter output stage provides fast discharging of load capacitance but rather slow charging. The opposite is obtained in the emitter-follower output stage shown in Fig. x8.6. Here, as v_I goes high, the transistor turns on and provides a low output resistance (characteristic of emitter followers), which results in fast charging of C_L. On the other hand, when v_I goes low, the transistor turns off and C_L is then left to discharge slowly through R_E.

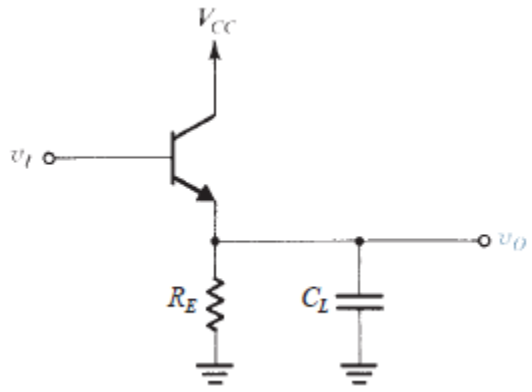

FIGURE x8.6 An emitter-follower output stage with capacitive load.

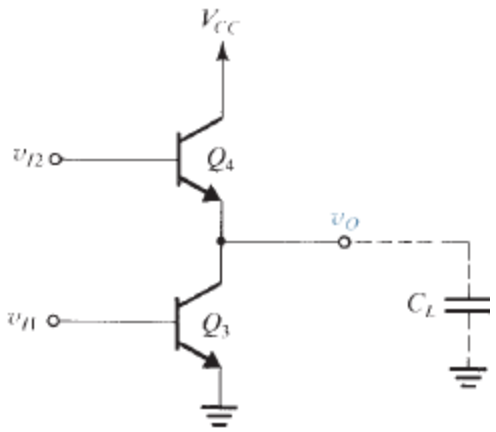

FIGURE x8.7 The totem-pole output stage.

It follows that an optimum output stage would be a combination of the common-emitter and the emitter-follower configurations. Such an output stage, shown in Fig. x8.7, has to be driven by two *complementary* signals v_{I1} and v_{I2}. When v_{I1} is high v_{I2} will be low, and in this case Q_3 will be on and saturated, and Q_4 will be off. The common-emitter transistor Q_3 will then provide the fast discharging of load capacitance and in steady state provide a low resistance (R_{CEsat}) to ground. Thus when the output is low, the gate can *sink* substantial amounts of current through the saturated transistor Q_3.

When v_{I1} is low and v_{I2} is high, Q_3 will be off and Q_4 will be conducting. The emitter follower Q_4 will then provide fast charging of load capacitance. It also provides the gate with a low output resistance in the high state and hence with the ability to *source* a substantial amount of load current.

Because of the appearance of the circuit in Fig. x8.7, with Q_4 stacked on top of Q_3, the circuit has been given the name **totem-pole output stage.** Also, because of the action of Q_4 in *pulling up* the output voltage to the high level, Q_4 is referred to as the **pull-up transistor.** Since the pulling up is achieved here by an active element (Q_4), the circuit is said to have an **active pull-up.** This is in contrast to the **passive pull-up** of RTL and DTL gates. Of course, the common-emitter transistor Q_3 provides the circuit with **active pull-down.** Finally, note that a special **driver circuit** is needed to generate the two complementary signals v_{I1} and v_{I2}.

Example x8.1

We wish to analyze the circuit shown together with its driving waveforms in Fig. x8.8 to determine the waveform of the output signal v_O. Assume that Q_3 and Q_4 have $\beta = 50$.

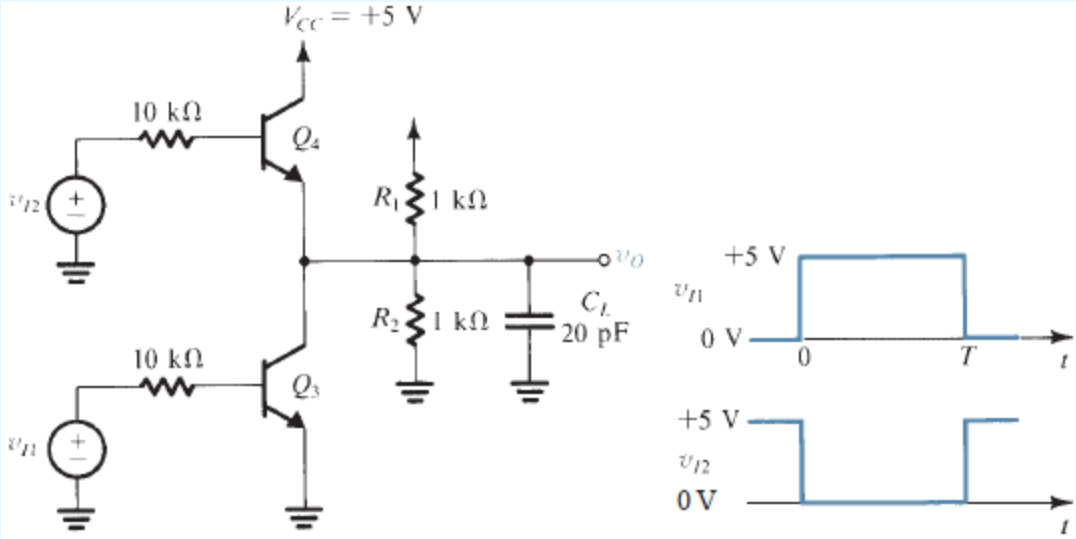

FIGURE x8.8 Circuit and input waveforms for Example x8.1.

Solution

Consider first the situation before v_{I1} goes high—that is, at time $t < 0$. In this case Q_3 is off and Q_4 is on, and the circuit can be simplified to that shown in Fig. x8.9. In this simplified circuit we have replaced the voltage divider (R_1, R_2) by its Thévenin equivalent. In the steady state, C_L will be charged to the output voltage v_O, whose value can be obtained as follows:

$$5 = 10 \times I_B + V_{BE} + I_E \times 0.5 + 2.5$$

Substituting $V_{BE} \simeq 0.7$ V and $I_B = I_E / (\beta + 1) = I_E / 51$ gives $I_E = 2.59$ mA. The output voltage v_O is given by

$$v_O = 2.5 + I_E \times 0.5 = 3.79 \text{ V}$$

We next consider the circuit as v_{I1} goes high and v_{I2} goes low. Transistor Q_3 turns on and transistor Q_4 turns off, and the circuit simplifies to that shown in Fig. x8.10. Again we have used the Thévenin equivalent of the divider (R_1, R_2). We shall also assume that the switching times of the transistors are negligibly small. Thus at $t = 0+$ the base current of Q_3 becomes

$$I_B = \frac{5 - 0.7}{10} = 0.43 \text{ mA}$$

Since at $t = 0$ the collector voltage of Q_3 is 3.79 V, and since this value cannot change instantaneously because of C_L, we see that at $t = 0+$ transistor Q_3 will be in the active mode. The collector current of Q_3 will be βI_B, which is 21.5 mA, and the circuit will have the equivalent shown in Fig. x8.11(a). A simpler version of this equivalent circuit, obtained using Thévenin's theorem, is shown in Fig. x8.11(b).

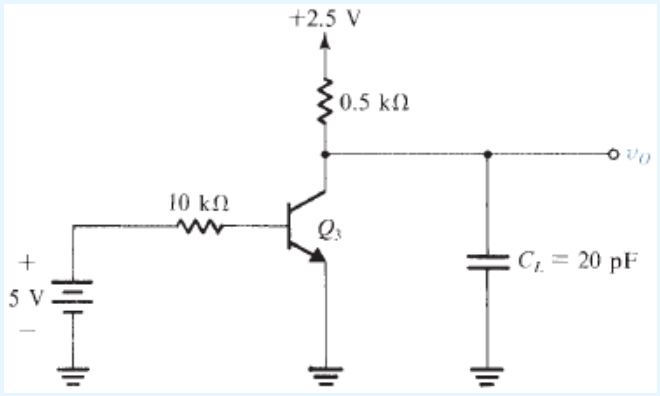

FIGURE x8.9 Circuit of Fig. x8.8 when Q_3 is off.

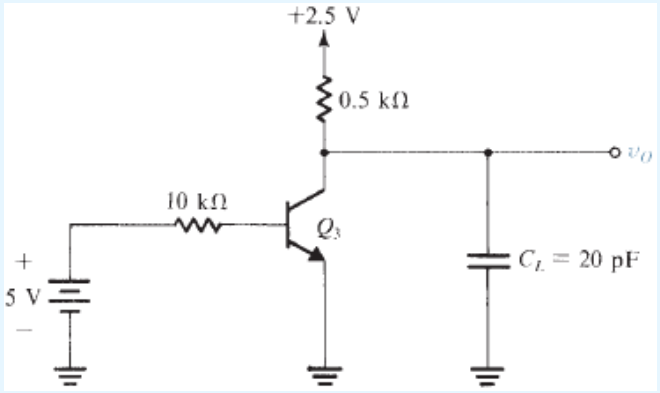

FIGURE x8.10 Circuit of Fig. x8.8 when Q_4 is off.

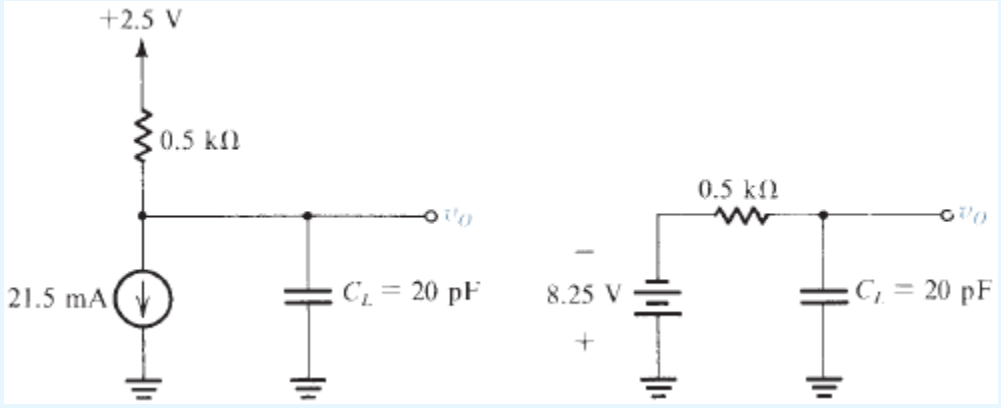

FIGURE x8.11 **(a)** Equivalent circuit for the circuit in Fig. x8.10 when Q_3 is in the active mode. **(b)** Simpler version of the circuit in (a) obtained using Thévenin's theorem.

The equivalent circuit of Fig. x8.11 applies as long as Q_3 remains in the active mode. This condition persists while C_L is being discharged and until v_O reaches about +0.3 V, at which time Q_3 enters saturation. This is illustrated by the waveform in Fig. x8.12. The time for the output voltage to fall from +3.79 V to +0.3 V, which can be considered the **fall time** t_f, can be obtained from

$$-8.25 - (-8.25 - 3.79)e^{-t_f/\tau} = 0.3$$

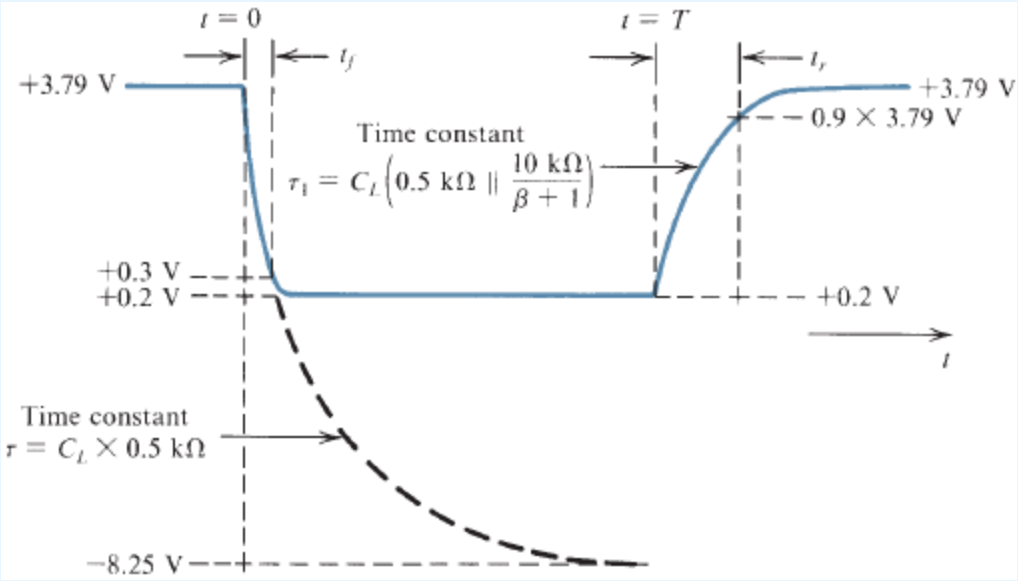

FIGURE x8.12 Details of the output voltage waveform for the circuit in Fig. x8.8.

which results in

$$t_f \simeq 0.34\tau$$

where

$$\tau = C_L \times 0.5\ \text{k}\Omega = 10\ \text{ns}$$

Thus $t_f = 3.4$ ns.

After Q_3 enters saturation, the capacitor discharges further to the final steady-state value of $V_{CE\text{sat}}$ ($\simeq 0.2$ V). The transistor model that applies during this interval is more complex; since the interval in question is quite short, we shall not pursue the matter further.

Consider next the situation as v_{I1} goes low and v_{I2} goes high at $t = T$. Transistor Q_3 turns off as Q_4 turns on. We assume that this occurs immediately, and thus at $t = T+$ the circuit simplifies to that in Fig. x8.9. We have already analyzed this circuit in the steady state, so we know that eventually v_O will reach +3.79 V. Thus v_O rises exponentially from +0.2 V toward +3.79 V with a time constant of $C_L\{0.5\ \text{k}\Omega//[10\ \text{k}\Omega/(\beta + 1)]\}$, where we have neglected the emitter resistance r_e. Denoting this time constant τ_1, we obtain $\tau_1 = 2.8$ ns. Defining the rise time t_r as the time for v_O to reach 90% of the final value, we obtain $3.79 - (3.79 - 0.2)e^{-tr/\tau 1} = 0.9 \times 3.79$, which results in $t_r = 6.4$ ns. Figure x8.12 illustrates the details of the output voltage waveform.

x8.1.5 The Complete Circuit of the TTL Gate

Figure x8.13 shows the complete TTL gate circuit. It consists of three stages: the input transistor Q_1, whose operation has already been explained, the driver stage Q_2, whose function is to generate the two complementary voltage signals required to drive the totem-pole circuit, which is the third (output) stage of the gate. The totem-pole circuit in the TTL gate has two additional components: the 130-Ω resistance in the collector circuit of Q_4 and the diode D in the emitter circuit of Q_4. The function of these two additional components will be explained shortly. Notice that the TTL gate is shown with only one

input terminal indicated. Inclusion of additional input terminals will be considered in Section x8.2 of the bonus materials

Because the driver stage Q_2 provides two complementary (that is, out-of-phase) signals, it is known as a **phase splitter.**

We shall now provide a detailed analysis of the TTL gate circuit in its two extreme states: one with the input high and one with the input low.

x8.1.6 Analysis When the Input Is High

When the input is high (say, +5 V), the various voltages and currents of the TTL circuit will have the values indicated in Fig. x8.14. The analysis illustrated in Fig. x8.14 is quite straightforward, and the order of the steps followed is indicated by the circled numbers. As expected, the input transistor is operating in the inverse active mode, and the input current, called the **input high current** I_{IH}, is small; that is,

$$I_{IH} = \beta_R I \simeq 15\ \mu\text{A}$$

where we assume that $\beta_R I \simeq 0.02$.

The collector current of Q_1 flows into the base of Q_2, and its value is sufficient to saturate the phase-splitter transistor Q_2. The latter supplies the base of Q_3 with sufficient current to drive it into saturation and lower its output voltage to $V_{CE\text{sat}}$ (0.1 to 0.2 V). The voltage at the collector of Q_2 is $V_{BE3} + V_{CE\text{sat}}(Q_2)$, which is approximately +0.9 V. If diode D were not included, this voltage would be sufficient to turn Q_4 on, which is contrary to the proper operation of the totem-pole circuit. Including diode D ensures that both Q_4 and D remain off. The saturated transistor Q_3 then establishes the low output voltage of the gate ($V_{CE\text{sat}}$) and provides a low impedance to ground.

In the low-output state the gate can sink a load current i_L, provided that the value of i_L does not exceed $\beta \times 2.6$ mA, which is the maximum collector current that Q_3 can sustain while remaining in saturation. Obviously the greater the value of i_L, the greater the output

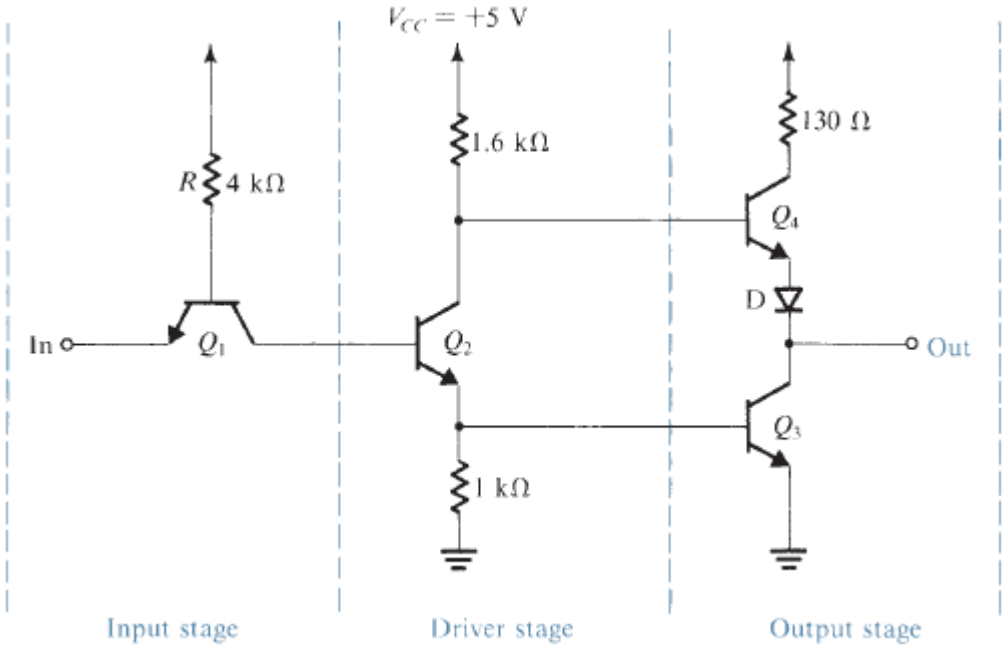

FIGURE x8.13 The complete TTL gate circuit with only one input terminal indicated.

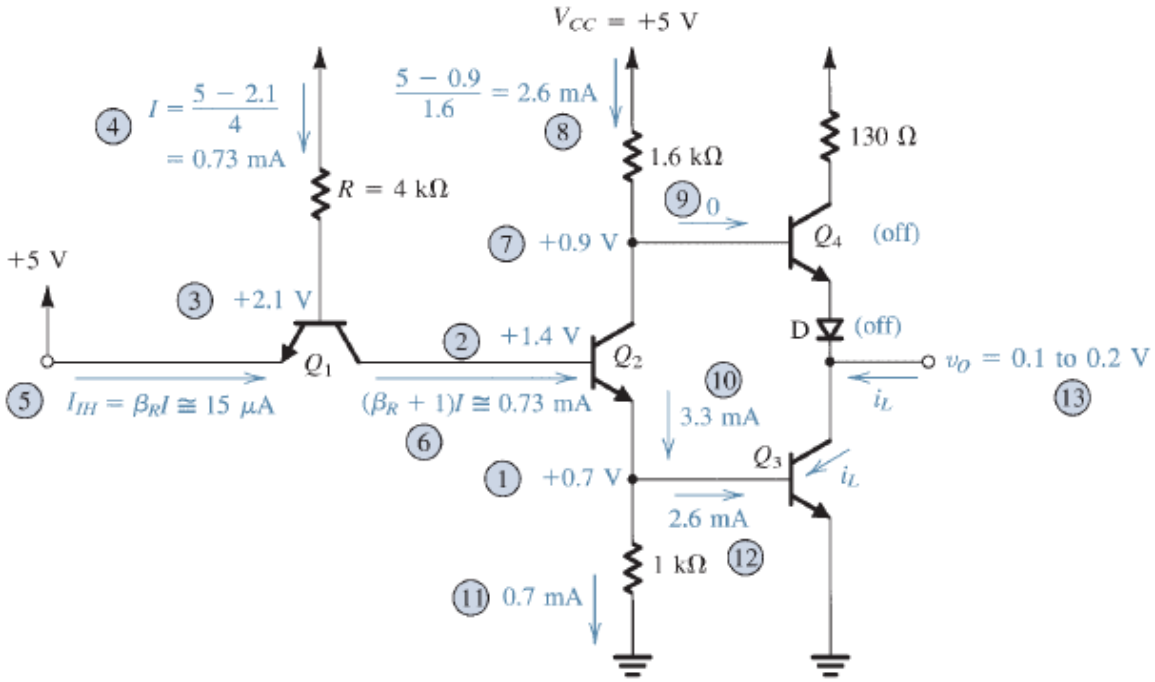

FIGURE x8.14 Analysis of the TTL gate with the input high. The circled numbers indicate the order of the analysis steps.

voltage will be. To maintain the logic-0 level below a certain specified limit, a corresponding limit has to be placed on the load current i_L. As will be seen shortly, it is this limit that determines the maximum fan-out of the TTL gate.

Figure x8.15 shows a sketch of the output voltage v_O versus the load current i_L of the TTL gate when the output is low. This is simply the v_{CE}–i_C characteristic curve of Q_3 measured with a base current of 2.6 mA. Note that at $i_L = 0$, v_O is the offset voltage, which is about 100 mV.

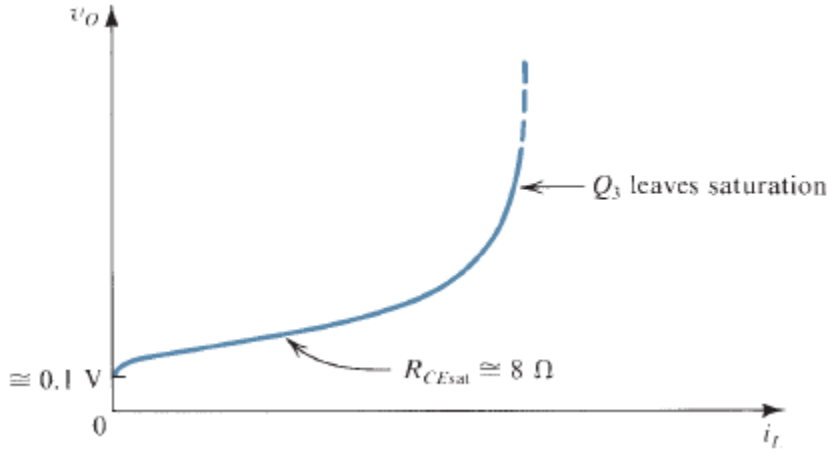

FIGURE x8.15 The v_O–i_L characteristic of the TTL gate when the output is low.

EXERCISE

x8.2 Assume that the saturation portion of the v_O–i_L characteristic shown in Fig. x8.15 can be approximated by a straight line (of slope = 8 Ω) that intersects the v_O axis at 0.1 V. Find the maximum load current that the gate is allowed to sink if the logic-0 level is specified to be ≤0.3 V.

Ans. 25 mA

x8.1.7 Analysis When the Input Is Low

Consider next the operation of the TTL gate when the input is at the logic-0 level (≃0.2 V). The analysis is illustrated in Fig. x8.16, from which we see that the base−emitter junction of Q_1 will be forward-biased and the base voltage will be approximately +0.9 V. Thus the current I can be found to be approximately 1 mA. Since 0.9 V is insufficient to forward-bias the series combination of the collector–base junction of Q1 and the base−emitter junction of Q_2 (at least 1.2 V would be required), the latter will be off. Therefore the collector current of Q1 will be almost zero and Q_1 will be saturated, with $V_{CE\text{sat}} \simeq 0.1$ V. Thus the base of Q_2 will be at approximately +0.3 V, which is indeed insufficient to turn Q_2 on.

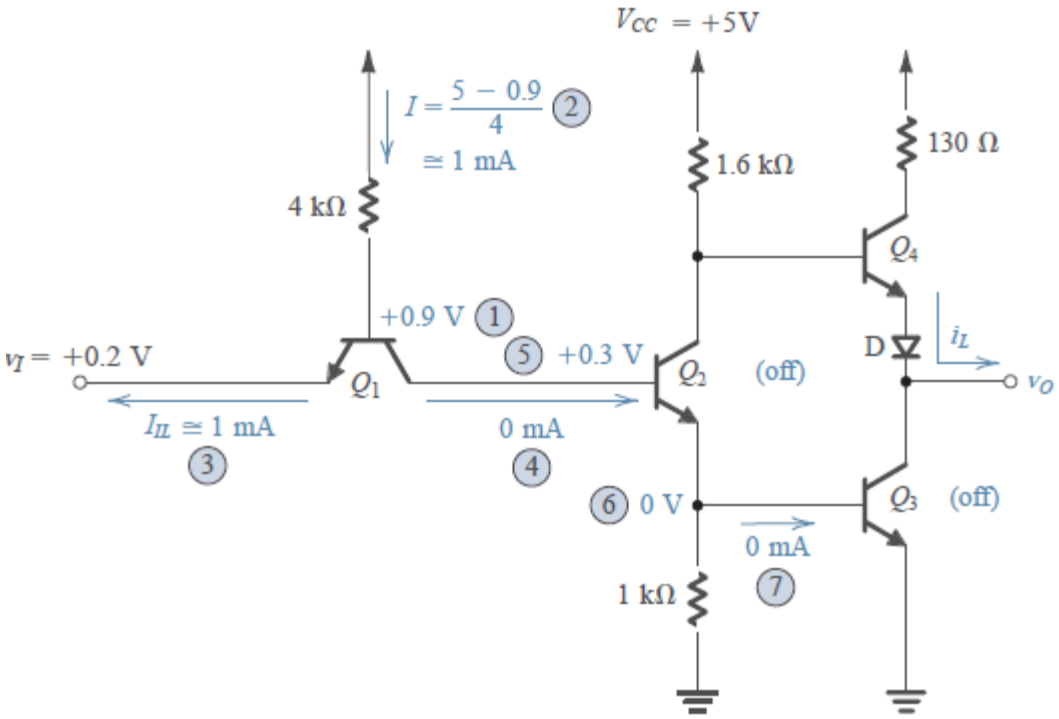

FIGURE x8.16 Analysis of the TTL gate when the input is low. The circled numbers indicate the order of the analysis steps.

The gate input current in the low state, called input-low current I_{IL}, is roughly equal to the current I ($\simeq$ 1 mA) and flows out of the emitter of Q_1. If the TTL gate is driven by another TTL gate, the output transistor Q_3 of the driving gate should sink this current I_{IL}. Since the output current that a TTL gate can sink is limited to a certain maximum value, the maximum fan-out of the gate is directly determined by the value of I_{IL}.

EXERCISES

x8.3 Consider the TTL gate analyzed in Exercise x8.2. Find its maximum allowable fan-out using the value of I_{IL} calculated above.

Ans. 25

x8.4 Find $V_{CE\text{sat}}$ of transistor Q_1 when the input of the gate is low (0.2 V). Assume that $\beta_F = 50$ and $\beta_R = 0.02$.

Ans. 98 mV

Let us continue with our analysis of the TTL gate. When the input is low, we see that both Q_2 and Q_3 will be off. Transistor Q_4 will be on and will supply (source) the load current i_L. Depending on the value of i_L, Q_4 will be either in the active mode or in the saturation mode.

With the gate output terminal open, the current i_L will be very small (mostly leakage) and the two junctions (base–emitter junction of Q_4 and diode D) will be barely conducting. Assuming that each junction has a 0.65-V drop and neglecting the voltage drop across the 1.6-kΩ resistance, we find that the output voltage will be

$$v_O \simeq 5 - 0.65 - 0.65 = 3.7 \text{ V}$$

As i_L is increased, Q_4 and D conduct more heavily, but for a range of i_L, Q_4 remains in the active mode, and v_O is given by

$$v_O = V_{CC} - \frac{i_L}{\beta + 1} \times 1.6 \text{ k}\Omega - V_{BE4} - V_D \tag{x8.1}$$

If we keep increasing i_L, a value will be reached at which Q_4 saturates. Then the output voltage becomes determined by the 130-Ω resistance according to the approximate relationship

$$v_O \simeq V_{CC} - i_L \times 130 - V_{CE\text{sat}}\,(Q_4) - V_D \tag{x8.2}$$

x8.1.8 Function of the 130-Ω Resistance

At this point the reason for including the 130-Ω resistance should be evident: It is simply to limit the current that flows through Q_4, especially in the event that the output terminal is accidentally short-circuited to ground. This resistance also limits the supply current in another circumstance, namely, when Q_4 turns on while Q_3 is still in saturation. To see how this occurs, consider the case where the gate input was high and then is suddenly brought down to the low level. Transistor Q_2 will turn off relatively fast because of the availability of a large reverse current supplied to its base terminal by the collector of Q_1. On the other hand, the base of Q_3 will have to discharge through the 1-k∧ resistance, and thus Q_3 will take some time to turn off. Meanwhile Q_4 will turn on, and a large current pulse will flow through the series combination of Q_4 and Q_3. Part of this current will serve the useful purpose of charging up any load capacitance to the logic-1 level. The magnitude of the current pulse will be limited by the 130-Ω resistance to about 30 mA.

The occurrence of these current pulses of short duration (called **current spikes**) raises another important issue. The current spikes have to be supplied by the V_{CC} source and, because of its finite source resistance, will result in voltage spikes (or "glitches") superimposed on V_{CC}. These voltage spikes could be coupled to other gates and flip-flops in the digital system and thus might produce false switching in other parts of the system. This effect, which might loosely be called **crosstalk,** is a problem in TTL systems. To reduce the size of the voltage spikes, capacitors (called bypass capacitors) should be connected between the supply rail and ground at frequent locations. These capacitors lower the impedance of the supply-voltage source and hence reduce the magnitude of the voltage spikes. Alternatively, one can think of the bypass capacitors as supplying the impulsive current spikes.

EXERCISES

x8.5 Assuming that Q_4 has $\beta = 50$ and that at the verge of saturation $V_{CE\text{sat}} = 0.3$ V, find the value of i_L at which Q_4 saturates.

Ans. 4.16 mA

x8.6 Assuming that at a current of 1 mA the voltage drops across the emitter−base junction of Q_4 and the diode D are each 0.7 V, find v_O when $i_L = 1$ mA and 10 mA. (Note the result of the previous exercise.)

Ans. 3.6 V; 2.7 V

x8.7 Find the maximum current that can be sourced by a TTL gate while the output high level (V_{OH}) remains greater than the minimum guaranteed value of 2.4 V.

Ans. 12.3 mA; or, more accurately, taking the base current of Q_4 into account, 13.05 mA

x8.2 CHARACTERISTICS OF STANDARD TTL

In this section we consider some of the important characteristics of standard TTL gates. Special improved forms of TTL will be dealt with in Section x8.3 of the bonus materials.

x8.2.1 Transfer Characteristic

Figure x8.17 shows the TTL gate together with a sketch of its voltage transfer characteristic drawn in a piecewise-linear fashion. The actual characteristic is, of course, a smooth curve. We shall now explain the transfer characteristic and calculate the various break-points and slopes. It will be assumed that the output terminal of the gate is open.

Segment *AB* is obtained when transistor Q_1 is saturated, Q_2 and Q_3 are off, and Q_4 and D are on. The output voltage is approximately two diode drops below V_{CC}. At point *B* the phase splitter (Q_2) begins to turn on because the voltage at its base reaches 0.6 V (0.5 V + V_{CEsat} of Q_1).

Over segment *BC*, transistor Q_1 remains saturated, but more and more of its base current *I* gets diverted to its base−collector junction and into the base of Q_2, which operates as a linear amplifier. Transistor Q_4 and diode D remain on, with Q_4 acting as an emitter follower. Meanwhile the voltage at the base of Q_3, although increasing, remains insufficient to turn Q_3 on (less than 0.6 V).

Let us now find the slope of segment *BC* of the transfer characteristic. Let the input v_I increase by an increment Δv_I. This increment appears at the collector of Q_1, since the saturated Q_1 behaves (approximately) as a three-terminal short circuit as far as signals are

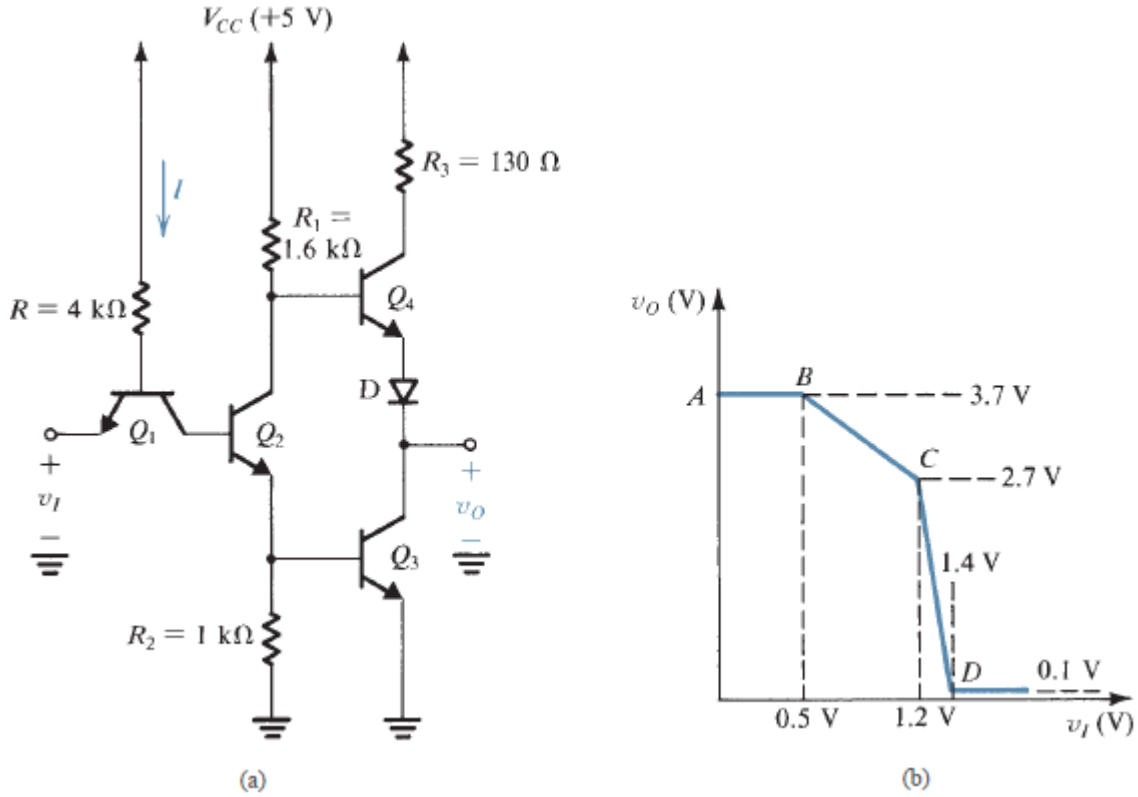

FIGURE x8.17 The TTL gate and its voltage transfer characteristic.

concerned. Thus at the base of Q_2 we have a signal Δv_I. Neglecting the loading of emitter follower Q_4 on the collector of Q_2, we can find the gain of the phase splitter from

$$\frac{v_{c2}}{v_{b2}} = \frac{-\alpha_2 R_1}{r_{e2} + R_2} \tag{x8.3}$$

The value of r_{e2} will obviously depend on the current in Q_2. This current will range from zero (as Q_2 begins to turn on) to the value that results in a voltage of about 0.6 V at the emitter of Q_2 (the base of Q_3). This value is about 0.6 mA and corresponds to point *C* on the transfer characteristic. Assuming an average current in Q_2 of 0.3 mA, we obtain $r_{e2} \simeq 83\ \Omega$. For $\alpha = 0.98$, the equation above results in a gain value of 1.45. Since the gain of the output follower Q_4 is close to unity, the overall gain of the gate, which is the slope of the *BC* segment, is about −1.45.

As already implied, breakpoint *C* is determined by Q_3 starting to conduct. The corresponding input voltage can be found from

$$\begin{aligned} v_I(C) &= V_{BE3} + V_{BE2} - V_{CE\text{sat}}(Q_1) \\ &= 0.6 + 0.7 - 0.1 = 1.2\ \text{V} \end{aligned}$$

At this point the emitter current of Q_2 is approximately 0.6 mA. The collector current of Q_2 is also approximately 0.6 mA; neglecting the base current of Q_4, the voltage at the collector of Q_2 is

$$v_{C2}\,(C) = 5 - 0.6 \times 1.6 \equiv 4\ \text{V}$$

Thus Q_2 is still in the active mode. The corresponding output voltage is

$$v_O\,(C) = 4 - 0.65 - 0.65 = 2.7\ \text{V}$$

As v_I is increased past the value of $v_I(C) = 1.2$ V, Q_3 begins to conduct and operates in the active mode. Meanwhile, Q_1 remains saturated, and Q_2 and Q_4 remain in the active mode. The circuit behaves as an amplifier until Q_2 and Q_3 saturate and Q_4 cuts off. This occurs at point *D* on the transfer characteristic, which corresponds to an input voltage $v_I(D)$ obtained from

$$\begin{aligned} v_I(D) &= V_{BE3} + V_{BE2} + V_{BC1} - V_{BE1} \\ &= 0.7 + 0.7 + 0.7 - 0.7 = 1.4\ \text{V} \end{aligned}$$

Note that we have in effect assumed that at point *D* transistor Q_1 is still saturated, but with $V_{CE\text{sat}} \simeq 0$. To see how this comes about, note that from point *B* on, more and more of the base current of Q_1 is diverted to its base−collector junction. Thus while the drop across the base−collector junction increases, that across the base−emitter junction decreases. At point *D* these drops become almost equal. For $v_I > v_I(D)$ the base−emitter junction of Q_1 cuts off; thus Q_1 leaves saturation and enters the inverse active mode.

Calculation of gain over the segment *CD* is a relatively complicated task. This is due to the fact that there are two paths from input to output: one through Q_3 and one through Q_4. A simple but gross approximation for the gain of this segment can be obtained from the coordinates of points *C* and *D* in Fig. x8.17(b), as follows:

$$\text{Gain} = -\frac{v_O(C) - v_O(D)}{v_I(D) - v_I(C)}$$
$$= -\frac{2.7 - 0.1}{1.4 - 1.2}$$
$$= -13 \text{ V/V}$$

From the transfer curve of Fig. x8.17(b) we can determine the critical points and the noise margins as follows: $V_{OH} = 3.7$ V; V_{IL} is somewhere in the range of 0.5 V to 1.2 V, and thus a conservative estimate would be 0.5 V; $V_{OL} = 0.1$ V; $V_{IH} = 1.4$ V; $NM_H = V_{OH} - V_{IH} = 2.3$ V; and $NM_L = V_{IL} - V_{OL} = 0.4$ V. It should be noted that these values are computed assuming that the gate is not loaded and without taking into account power-supply or temperature variations.

EXERCISE

x8.8 Taking into account the fact that the voltage across a forward-biased *pn* junction changes by about −2 mV/°C, find the coordinates of points *A*, *B*, *C*, and *D* of the gate transfer characteristic at −55°C and at +125°C. Assume that the characteristic in Fig. x8.17(b) applies at 25°C, and neglect the small temperature coefficient of $V_{CE\,sat}$.

Ans. At −55°C: (0, 3.38), (0.66, 3.38), (1.52, 2.16), (1.72, 0.1); at +125°C: (0, 4.1), (0.3, 4.1), (0.8, 3.46), (1.0, 0.1)

x8.2.2 Manufacturers' Specifications

Manufacturers of TTL usually provide curves for the gate transfer characteristic, the input *i*–*v* characteristic, and the output *i*–*v* characteristic, measured at the limits of the specified operating temperature range. In addition, guaranteed values are usually given for the parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH}. For standard TTL (known as the 74 series) these values are $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V, $V_{IL} = 0.8$ V, and $V_{IH} = 2$ V. These limit values are guaranteed for a specified tolerance in power-supply voltage and for a maximum fan-out of 10. From our discussion in Section x8.1 of the bonus materials we know that the maximum fan-out is determined by the maximum current that Q_3 can sink while remaining in saturation and while maintaining a saturation voltage lower than a guaranteed maximum ($V_{OL} = 0.4$ V). Calculations performed in Section x8.1 of the bonus materials indicate the possibility of a maximum fan-out of 20 to 30. Thus the figure specified by the manufacturer is appropriately conservative.

The parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH} can be used to compute the noise margins as follows:

$$NM_H = V_{OH} - V_{IH} = 0.4 \text{ V}$$
$$NM_L = V_{IL} - V_{OL} = 0.4 \text{ V}$$

EXERCISES

x8.9 In Section x8.1 of the bonus materials we found that when the gate input is high, the base current of Q_3 is approximately 2.6 mA. Assume that this value applies at 25°C and that at this temperature $V_{BE} \simeq 0.7$ V. Taking into account the −2-mV/°C temperature coefficient of V_{BE} and neglecting all other changes, find the base current of Q_3 at −55°C and at +125°C.

Ans. 2.2 mA; 3 mA

x8.10 Figure xE8.10 shows sketches of the i_L–v_O characteristics of a TTL gate when the output is low. Use these characteristics together with the results of Exercise x8.9 to calculate the value of β of transistor Q_3 at −55°C, +25°C, and +125°C.

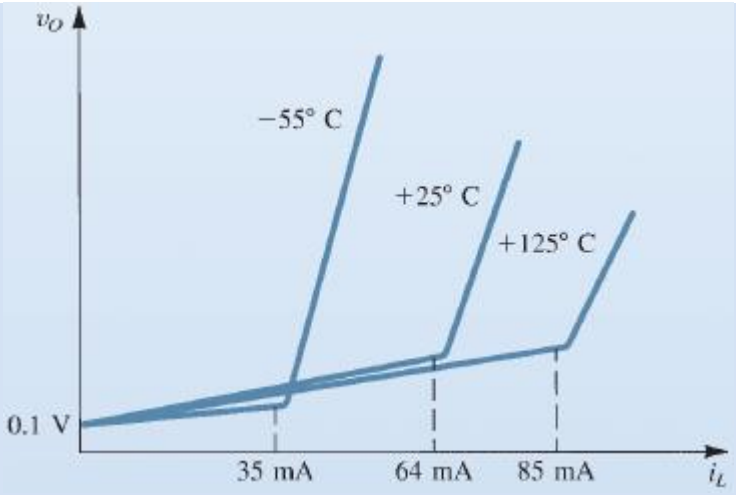

FIGURE xE8.10

Ans. 16; 25; 28

x8.2.3 Propagation Delay

The propagation delay of TTL gates is defined conventionally as the time between the 1.5-V points of corresponding edges of the input and output waveforms. For standard TTL (also known as *medium-speed* TTL) t_P is typically about 10 ns.

As far as power dissipation is concerned it can be shown (see Exercise x8.11) that when the gate output is high the gate dissipates 5 mW, and when the output is low the dissipation is 16.7 mW. Thus the average dissipation is 11 mW, resulting in a delay-power product of about 100 pJ.

EXERCISE

x8.11 Calculate the value of the supply current (I_{CC}), and hence the power dissipated in the TTL gate, when the output terminal is open and the input is (a) low at 0.2 V (see Fig. x8.16) and (b) high at +5 V (see Fig. x8.14).

Ans. (a) 1 mA, 5 mW; (b) 3.33 mA, 16.7 mW

x8.2.4 Dynamic Power Dissipation

In Section x8.1 of the bonus materials the occurrence of supply current spikes was explained. These spikes give rise to additional power drain from the V_{CC} supply. This **dynamic power** is also dissipated in the gate circuit. It can be evaluated by multiplying the average current due to the spikes by V_{CC}, as illustrated by the solution of Exercise x8.12.

EXERCISE

x8.12 Consider a TTL gate that is switched on and off at the rate of 1 MHz. Assume that each time the gate is turned off (that is, the output goes high) a supply-current pulse of 30-mA amplitude and 2-ns width occurs. Also assume that no current spike occurs when the gate is turned on. Calculate the average supply current due to the spikes, and the dynamic power dissipation.

Ans. 60 μA; 0.3 mW

x8.2.5 The TTL NAND Gate

Figure x8.18 shows the basic TTL gate. Its most important feature is the **multiemitter transistor** Q_1 used at the input. Figure x8.19 shows the structure of the multiemitter transistor.

It can be easily verified that the gate of Fig. x8.18 performs the NAND function. The output will be high if one (or both) of the inputs is (are) low. The output will be low in only one case: when both inputs are high. Extension to more than two inputs is straightforward and is achieved by diffusing additional emitter regions.

Although theoretically an unused input terminal may be left open-circuited, this is generally not a good practice. An open-circuit input terminal acts as an "antenna" that "picks up" interfering signals and thus could cause erroneous gate switching. An unused input terminal should therefore be connected to the positive power supply *through a resistance* (of, say, 1 kΩ). In this way the corresponding base–emitter junction of Q_1 will be reverse-biased and thus will have no effect on the operation of the gate. The series resistance is included in order to limit the current in case of breakdown of the base–emitter junction due to transients on the power supply.

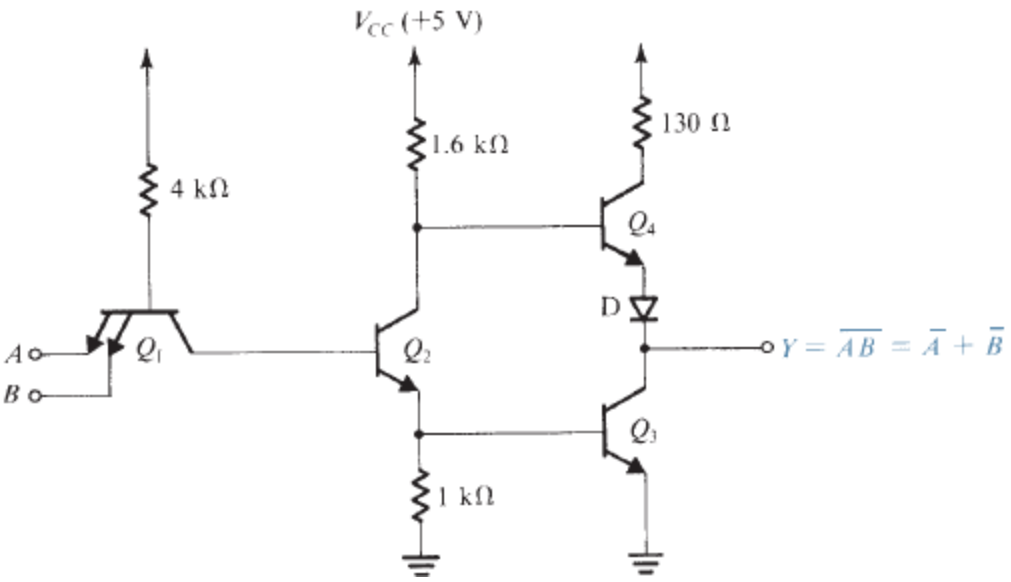

FIGURE x8.18 The TTL NAND gate.

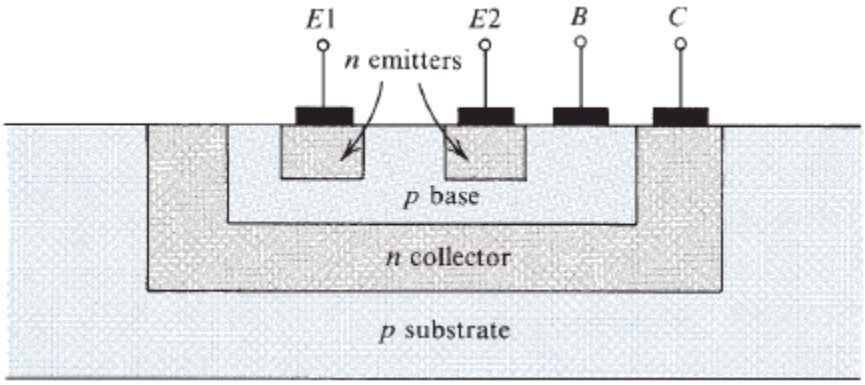

FIGURE x8.19 Structure of the multiemitter transistor Q_1.

x8.2.6 Other TTL Logic Circuits

On a TTL MSI chip there are many cases in which logic functions are implemented using "stripped-down" versions of the basic TTL gate. As an example we show in Fig. x8.20 the TTL implementation of the AND-OR-INVERT function. As shown, the phase-splitter transistors of two gates are connected in parallel, and a single output stage is used. The reader is urged to verify that the logic function realized is as indicated.

At this point it should be noted that the totem-pole output stage of TTL does *not* allow connecting the output terminals of two gates to realize the AND function of their outputs (known as the wired-AND connection). To see the reason for this, consider two gates whose outputs are connected together, and let one gate have a high output and the other have a low output. Current will flow from Q_4 of the first gate through Q_3 of the second gate. The current value will fortunately be limited by the 130-Ω resistance. Obviously, however, no useful logic function is realized by this connection.

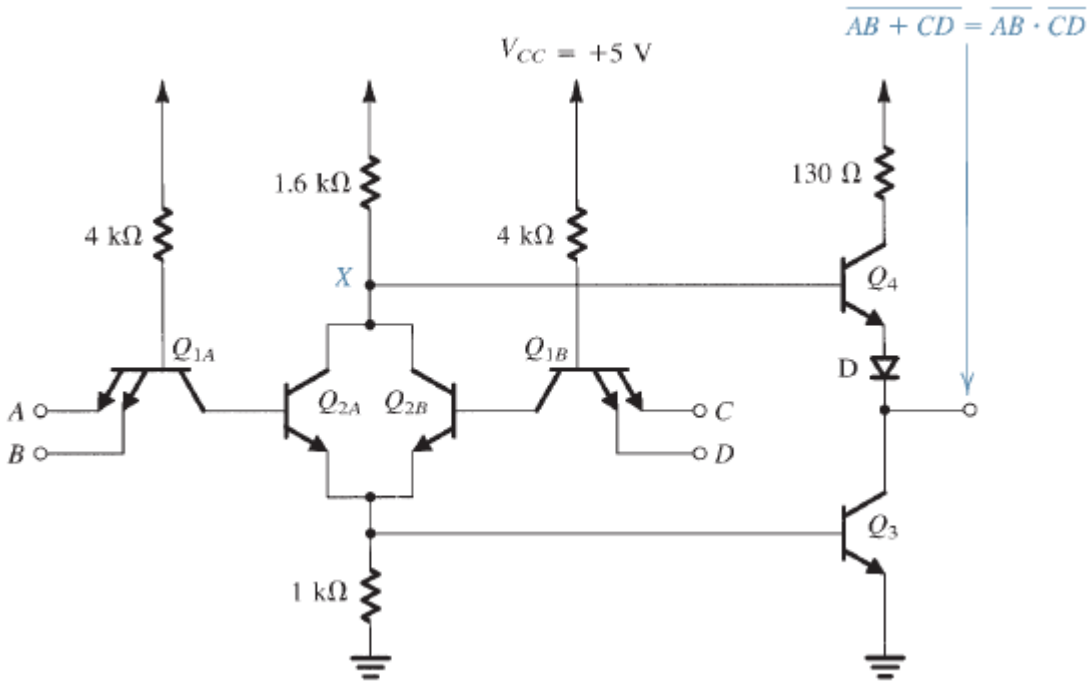

FIGURE x8.20 A TTL AND-OR-INVERT gate.

The lack of wired-AND capability is a drawback of TTL. Nevertheless, the problem is solved in a number of ways, including doing the paralleling at the phase-splitter stage, as illustrated in Fig. x8.20. Another solution consists of deleting the emitter-follower transistor altogether. The result is an output stage consisting solely of the common-emitter transistor Q_3 without even a collector resistance. Obviously, one can connect the outputs of such gates together to a common collector resistance and achieve a wired-AND capability. TTL gates of this type are known as **open-collector TTL.** The obvious disadvantage is the slow rise time of the output waveform.

Another useful variant of TTL is the **tristate** output arrangement explored in Exercise x8.13.

Tristate TTL enables the connection of a number of TTL gates to a common output line (or *bus*). At any particular time the signal on the bus will be determined by the one TTL gate that is *enabled* (by raising its third-state input terminal). All other gates will be in the third state and thus will have no control of the bus.

EXERCISE

x8.13 The circuit shown in Fig. xE8.13 is called tristate TTL. Verify that when the terminal labeled Third state is high, the gate functions normally and that when this terminal is low, both transistors Q_3 and Q_4 cut off and the output of the gate is an open circuit. The latter state is the third state, or the high-output impedance state.

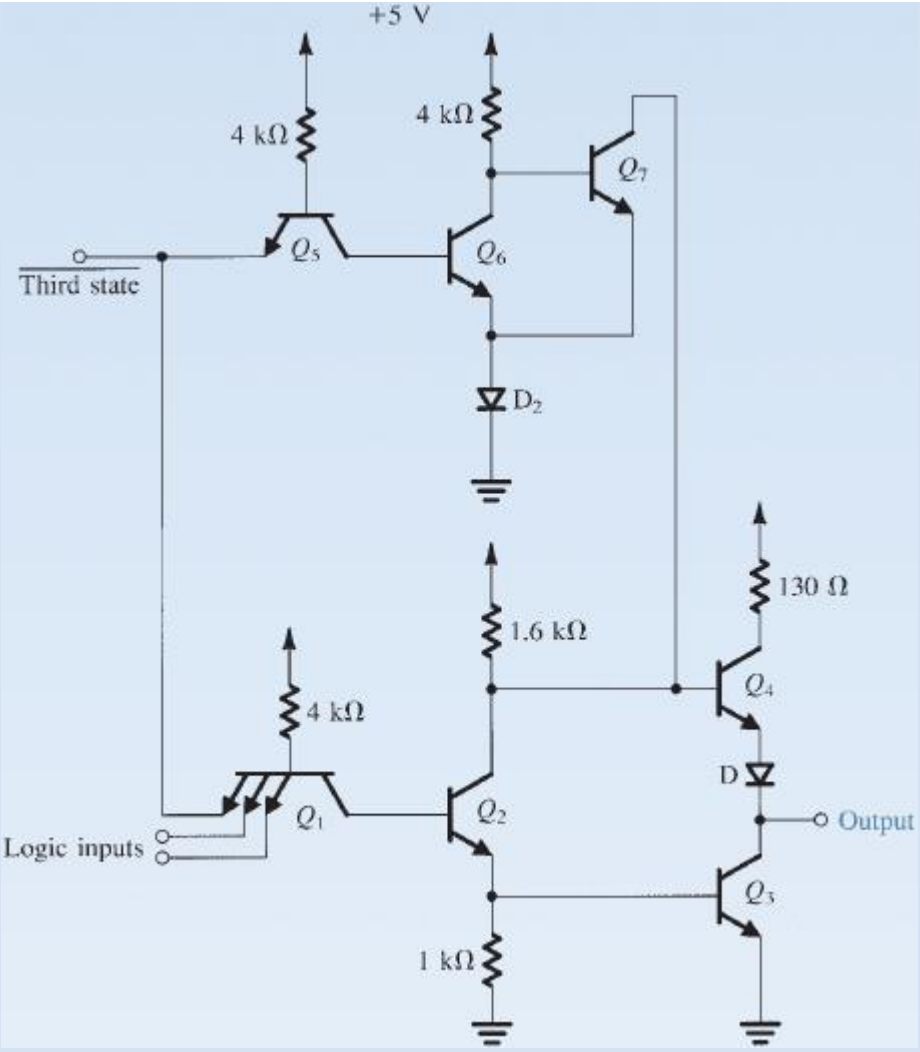

FIGURE xE8.13

x8.3 TTL Families with Improved Performance

The standard TTL circuits studied in the two previous sections were introduced in the mid-1960s. Since then, several improved versions have been developed. In this section we shall discuss some of these improved TTL subfamilies. As will be seen the improvements are in two directions: increasing speed and reducing power dissipation.

The speed of the standard TTL gate of Fig. x8.18 is limited by two mechanisms: first, transistors Q_1, Q_2, and Q_3 saturate, and hence we have to contend with their finite storage time. Although Q_2 is discharged reasonably quickly because of the active mode of operation of Q_1, as already explained, this is not true for Q_3, whose base charge has to leak out through the 1-kΩ resistance in its base circuit. Second, the resistances in the circuit, together with the various transistor and wiring capacitances, form relatively long time constants, which contribute to lengthening the gate delay.

It follows that there are two approaches to speeding up the operation of TTL. The first is to prevent transistor saturation and the second is to reduce the values of all resistances. Both approaches are utilized in the Schottky TTL circuit family.

x8.3.1 Schottky TTL

In Schottky TTL, transistors are prevented from saturation by connecting a low-voltage drop diode between base and collector, as shown in Fig. x8.21. These diodes, formed as a metal-to-semiconductor junction, are called Schottky diodes and have a forward voltage drop of about 0.5 V. Schottky diodes are easily fabricated and do not increase chip area. In fact, the Schottky TTL fabrication process has been designed to yield transistors with smaller areas and thus higher β and f_T than those produced by the standard TTL process. Figure x8.21 also shows the symbol used to represent the combination of a transistor and a Schottky diode, referred to as a Schottky transistor.

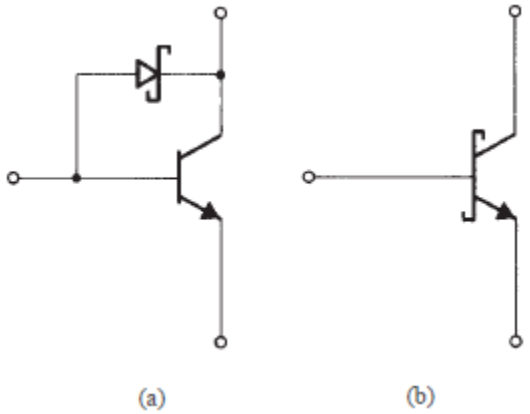

FIGURE x8.21 **(a)** A transistor with a Schottky diode clamp. **(b)** Circuit symbol for the connection in (a), known as a Schottky transistor.

x8.4 Emitter-Coupled Logic (ECL)

Emitter-coupled logic (ECL) was the fastest logic circuit family available for conventional logic-system design, until the emergence of CMOS technologies. High speed is achieved by operating all bipolar transistors out of saturation, thus avoiding storage-time delays, and by keeping the logic signal swings relatively small (about 0.8 V or less), thus reducing the time required to charge and discharge the various load and parasitic capacitances. Saturation in ECL is avoided by using the BJT differential pair as a current switch. The BJT differential pair was studied in Chapter 6 of the eighth edition.

x8.4.1 The Basic Principle

Emitter-coupled logic is based on the use of a current-steering switch introduced in Section 16.2 of the eighth edition. Such a switch can be most conveniently realized using the differential pair shown in Fig. x8.22. The pair is biased with a constant-current source I, and one side is connected to a reference voltage V_R. The current I can be steered to either Q_1 or Q_2 under the control of the input signal v_I . Specifically, when v_I is greater than V_R by about $4V_T$ ($\simeq$100 mV), nearly all the current I is conducted by Q_1, and thus for

$\alpha_1 \simeq 1$, $v_{O1} = V_{CC} - IR_C$. Simultaneously, the current through Q_2 will be nearly zero, and thus $v_{O2} = V_{CC}$. Conversely, when v_I is lower than V_R by about $4V_T$, most of the current I will flow through Q_2, and the current through Q_1 will be nearly zero. Thus $v_{O1} = V_{CC}$ and $v_{O2} = V_{CC} - IR_C$.

The preceding description suggests that as a logic element, the differential pair realizes an inversion function at v_{O1} and simultaneously provides the complementary output signal at v_{O2}. The output logic levels are $V_{OH} = V_{CC}$ and $V_{OL} = V_{CC} - IR_C$, and thus the output logic swing is IR_C. A number of additional remarks can be made concerning this circuit:

1. The differential nature of the circuit makes it less susceptible to picked-up noise. In particular, an interfering signal will tend to affect both sides of the differential pair similarly and thus will not result in current switching. This is the common-mode rejection property of the differential pair (see Section 9.2).
2. The current drawn from the power supply remains constant during switching. Thus, unlike CMOS (and TTL), no supply current spikes occur in ECL, eliminating an important source of noise in digital circuits. This is a definite advantage, especially since ECL is usually designed to operate with small signal swings and has correspondingly low noise margins.
3. The output signal levels are both referenced to V_{CC} and thus can be made particularly stable by operating the circuit with $V_{CC} = 0$: in other words, by utilizing a negative power supply and connecting the V_{CC} line to ground. In this case, $V_{OH} = 0$ and $V_{OL} = -IR_C$.
4. Some means must be provided to make the output signal levels compatible with those at the input so that one gate can drive another. As we shall see shortly, practical ECL gate circuits incorporate a level-shifting arrangement that serves to center the output signal levels on the value of V_R.
5. The availability of complementary outputs considerably simplifies logic design with ECL.

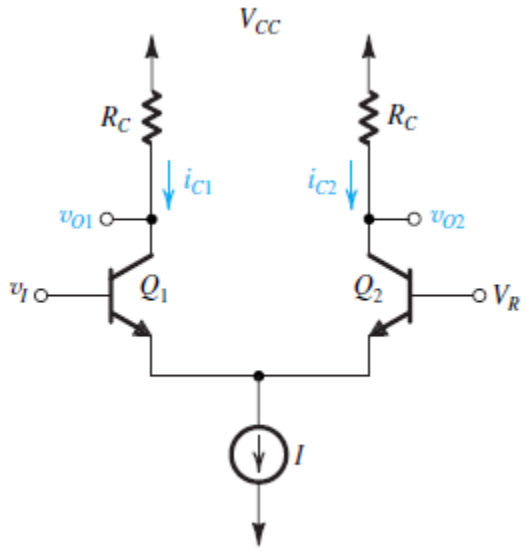

Figure x8.22 The basic element of ECL is the differential pair. Here, V_R is a reference voltage.

EXERCISE

x8.14 For the circuit in Fig. x8.22, let $V_{CC} = 0$, $I = 4$ mA, $R_C = 220\Omega$, $V_R = -1.32$ V, and assume $\alpha \simeq 1$. Determine V_{OH} and V_{OL}. By how much should the output levels be shifted so that the values of V_{OH} and V_{OL} become centered on V_R? What will the shifted values of V_{OH} and V_{OL} be?

Ans. 0; –0.88 V; –0.88 V; –0.88 V, –1.76 V

x8.4.2 ECL Families

Currently there are two popular forms of commercially available ECL—namely, ECL 10K and ECL 100K. The ECL 100K series features gate delays on the order of 0.75 ns and dissipates about 40 mW/gate, for a delay–power product of 30 pJ. Although its power dissipation is relatively high, the 100K series provides the shortest available gate delay in small- and medium-scale integrated circuit packages.

The ECL 10 K series is slightly slower; it features a gate propagation delay of 2 ns and a power dissipation of 25 mW for a delay–power product of 50 pJ. Although the value of *PDP* is higher than that obtained in the 100K series, the 10K series is easier to use. This is because the rise and fall times of the pulse signals are deliberately made longer, thus reducing signal coupling, or cross talk, between adjacent signal lines. ECL 10K has an "edge speed" of about 3.5 ns, compared with the approximately 1 ns of ECL 100K. To give concreteness to our study of ECL, in the following we shall consider the popular ECL 10K in some detail. The same techniques, however, can be applied to other types of ECL.

In addition to its usage in SSI and MSI circuit packages, ECL is also employed in large-scale and VLSI applications. A variant of ECL known as **current-mode logic** (CML) is utilized in VLSI applications (see Treadway, 1989, and Wilson, 1990).

x8.4.3 The Basic Gate Circuit

The basic gate circuit of the ECL 10K family is shown in Fig. x8.23. The circuit consists of three parts. The network composed of Q_1, D_1, D_2, R_1, R_2, and R_3 generates a reference voltage V_R whose value at room temperature is –1.32 V. As will be shown, the value of this reference voltage is made to change with temperature in a predetermined manner to keep the noise margins almost constant. Also, the reference voltage V_R is made relatively insensitive to variations in the power-supply voltage V_{EE}.

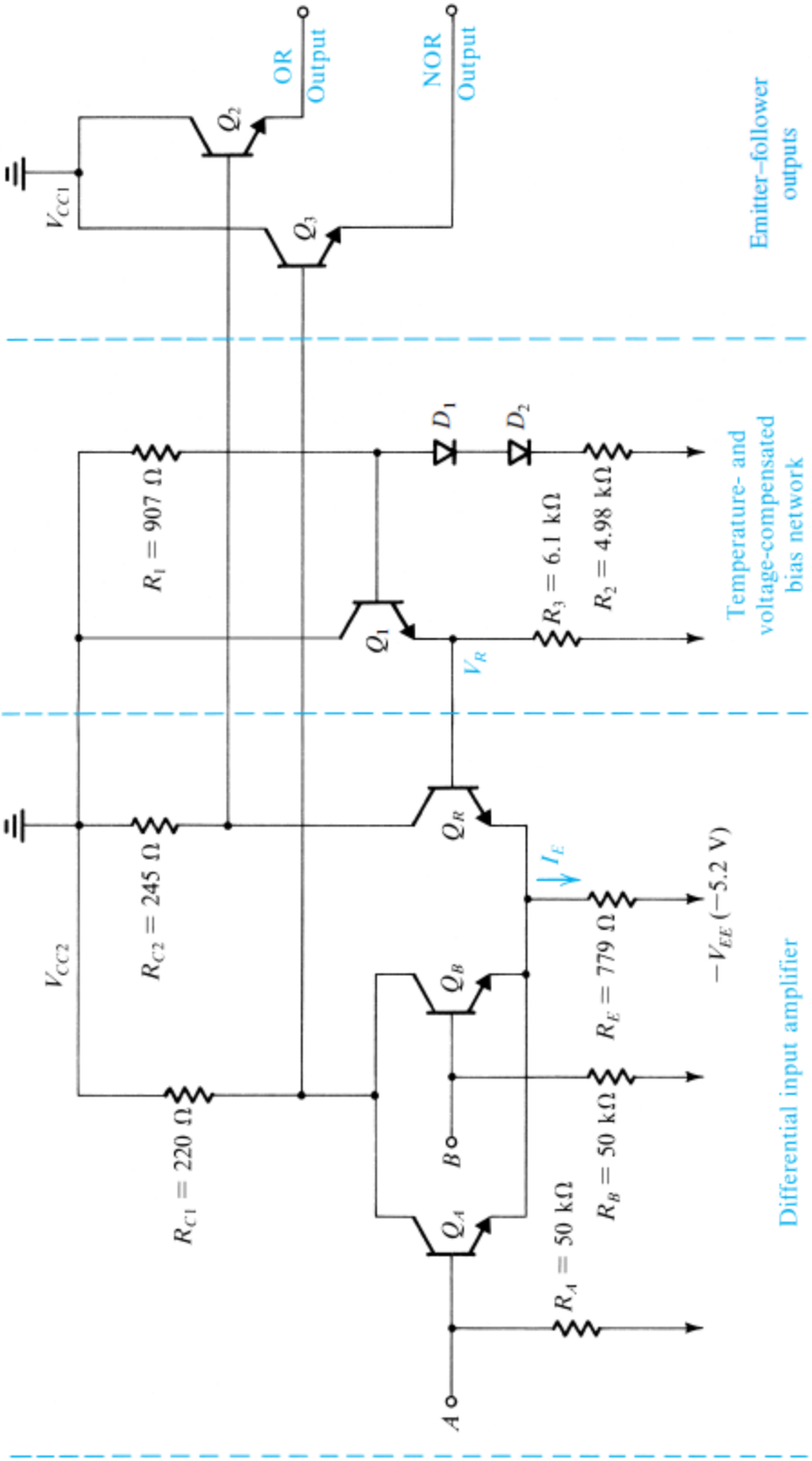

Figure x8.23 Basic circuit of the ECL 10K logic-gate family.

EXERCISE

x8.15 Figure xE8.15 shows the circuit that generates the reference voltage V_R. Assuming that the voltage drop across each of D_1, D_2, and the base–emitter junction of Q_1 is 0.75 V, calculate the value of V_R. Neglect the base current of Q_1.

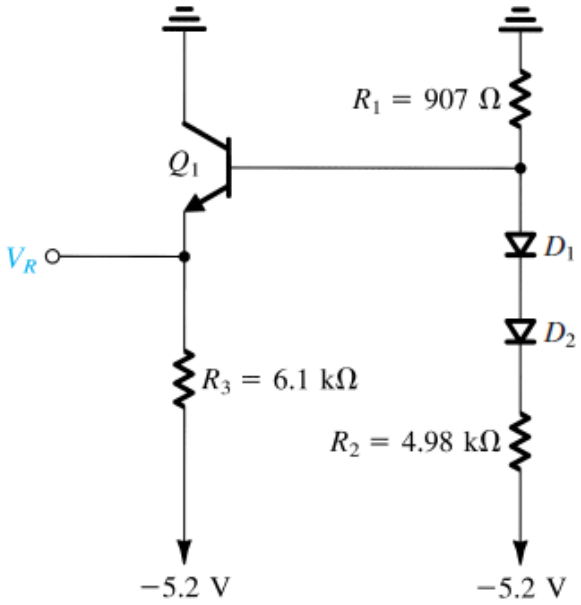

Figure xE8.15

Ans. –1.32 V

The second part, and the heart of the gate, is the differential amplifier formed by Q_R and either Q_A or Q_B. This differential amplifier is biased not by a constant-current source, as was done in the circuit of Fig. x8.22, but with a resistance R_E connected to the negative supply $-V_{EE}$. Nevertheless, we will shortly show that the current in R_E remains approximately constant over the normal range of operation of the gate. One side of the differential amplifier consists of the reference transistor Q_R, whose base is connected to the reference voltage V_R. The other side consists of a number of transistors (two in the case shown), connected in parallel, with separated bases, each connected to a gate input. If the voltages applied to A and B are at the logic-0 level, which, as we will soon find out, is about 0.4 V below V_R, both Q_A and Q_B, will be off and the current I_E in R_E will flow through the reference transistor Q_R. The resulting voltage drop across R_{C2} will cause the collector voltage of Q_R to be low.

On the other hand, when the voltage applied to A or B is at the logic-1 level, which, as we will show shortly, is about 0.4 V above V_R, transistor Q_A or Q_B, or both, will be on and Q_R will be off. Thus the current I_E will flow through Q_A or Q_B, or both, and an almost equal current will flow through R_{C1}. The resulting voltage drop across R_{C1} will cause the collector voltage to drop. Meanwhile, since Q_R is off, its collector voltage rises. We thus see that the voltage at the collector of Q_R will be high if A or B, or both, is high, and thus

at the collector of Q_R, the OR logic function, $A + B$, is realized. On the other hand, the common collector of Q_A and Q_B will be high only when A and B are simultaneously low. Thus at the common collector of Q_A and Q_B, the logic function $\overline{AB} = \overline{A + B}$ is realized. We therefore conclude that the two-input gate of Fig. x8.23 realizes the OR function and its complement, the NOR function. The availability of complementary outputs is an important advantage of ECL; it simplifies logic design and avoids the use of additional inverters with associated time delay.

It should be noted that the resistance connecting each of the gate input terminals to the negative supply enables the user to leave an unused input terminal open: An open input terminal will be *pulled down* to the negative supply voltage, and its associated transistor will be off.

EXERCISE

x8.16 With input terminals A and B in Fig. x8.23 left open, find the current I_E through R_E. Also find the voltages at the collector of Q_R and at the common collector of the input transistors Q_A and Q_B. Use $V_R = -1.32$ V, V_{BE} of $Q_R \simeq 0.75$ V, and assume that β of Q_R is very high.

Ans. 4 mA; –1 V; 0 V

The third part of the ECL gate circuit is composed of the two emitter followers, Q_2 and Q_3. The emitter followers do not have on-chip loads, since in many applications of high-speed logic circuits the gate output drives a transmission line terminated at the other end, as indicated in Fig. x8.24.

The emitter followers have two purposes: First, they shift the level of the output signals by one V_{BE} drop. Thus, using the results of Exercise x8.16, we see that the output levels become approximately –1.75 V and –0.75 V. These shifted levels are centered approximately around the reference voltage ($V_R = -1.32$ V), which means that one gate can drive another. This compatibility of logic levels at input and output is an essential requirement in the design of gate circuits.

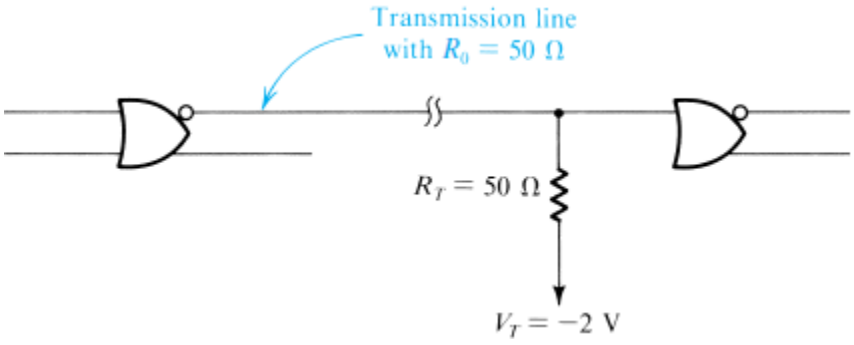

Figure x8.24 The proper way to connect high-speed logic gates such as ECL. Properly terminating the transmission line connecting the two gates eliminates the "ringing" that would otherwise corrupt the logic signals.

The second function of the output emitter followers is to provide the gate with low output resistances and with the large output currents required for charging load capacitances. Since these large transient currents can cause spikes on the power-supply line, the collectors of the emitter followers are connected to a power-supply terminal V_{CC1} separate from that of the differential amplifier and the reference-voltage circuit, V_{CC2}. Here we note that the supply current of the differential amplifier and the reference circuit remains almost constant. The use of separate power-supply terminals prevents the coupling of power-supply spikes from the output circuit to the gate circuit and thus lessens the likelihood of false gate switching. Both V_{CC1} and V_{CC2} are of course connected to the same system ground, external to the chip.

x8.4.4 Voltage-Transfer Characteristics

Having provided a qualitative description of the operation of the ECL gate, we shall now derive its voltage-transfer characteristics. This will be done under the conditions that the outputs are terminated in the manner indicated in Fig. x8.24. Assuming that the *B* input is low and thus Q_B is off, the circuit simplifies to that shown in Fig. x8.25. We wish to analyze this circuit to determine v_{OR} versus v_I and v_{NOR} versus v_I (where $v_I \equiv v_A$).

In the analysis to follow we shall make use of the exponential i_C–v_{BE} characteristic of the BJT. Since the BJTs used in ECL circuits have small areas (in order to have small capacitances and hence high f_T), their scale currents I_S are small. We will therefore assume that at an emitter current of 1 mA, an ECL transistor has a V_{BE} drop of 0.75 V.

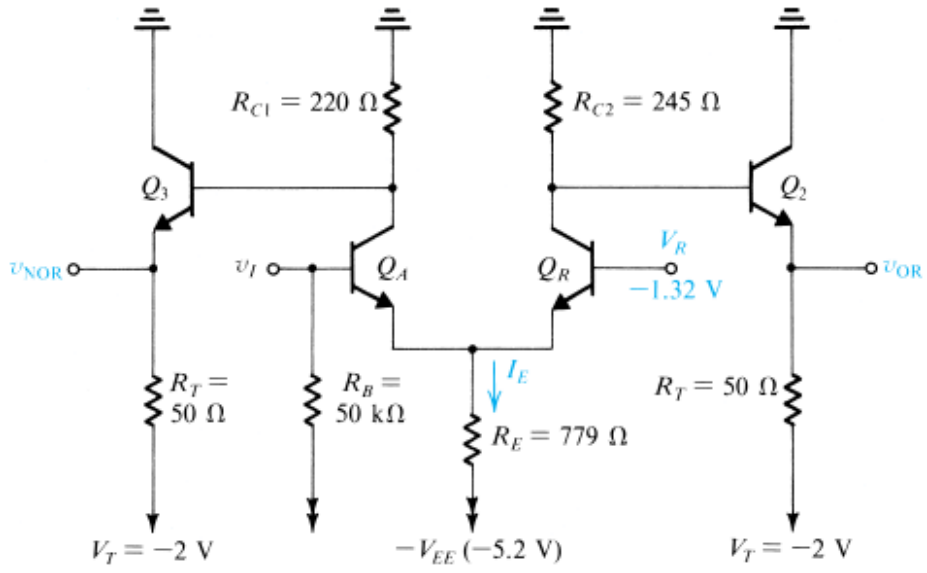

Figure x8.25 Simplified version of the ECL gate for the purpose of finding transfer characteristics.

The OR Transfer Curve Figure x8.26 is a sketch of the OR transfer characteristic, v_{OR} versus v_I, with the parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH} indicated. However, to simplify the calculation of V_{IL} and V_{IH}, we shall use an alternative to the unity-gain definition. Specifically, we shall assume that at point *x*, transistor Q_A is conducting 1% of I_E while Q_R is conducting 99% of I_E. The reverse will be assumed for point *y*. Thus at point *x* we have

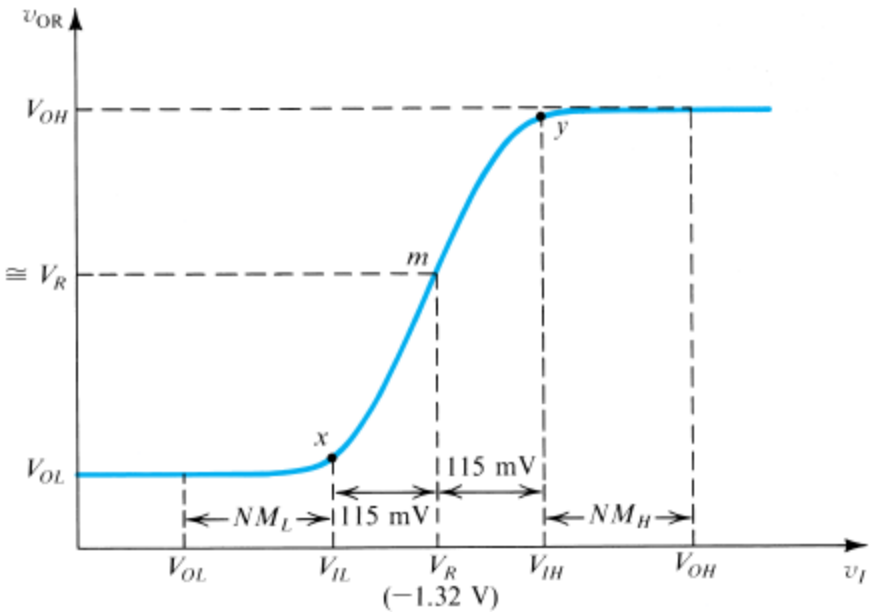

Figure x8.26 The OR transfer characteristic v_{OR} versus v_I, for the circuit in Fig. x8.25.

$$\frac{V_{BE}|_{Q_R}}{I_E|_{Q_A}} = 99$$

Using the exponential i_E–v_{BE} relationship, we obtain

$$V_{BE}|_{Q_R} - V_{BE}|_{Q_A} = V_T \ln 99 = 115 \text{ mV}$$

which gives

$$V_{IL} = -1.32 - 0.115 = -1.435 \text{ V}$$

Assuming Q_A and Q_R to be matched, we can write

$$V_{IH} - V_R = V_R - V_{IL}$$

which can be used to find V_{IH} as

$$V_{IH} = -1.205 \text{ V}$$

To obtain V_{OL}, we note that Q_A is off and Q_R carries the entire current I_E, given by

$$\begin{aligned} I_E &= \frac{V_R - V_{BE}|_{Q_R} + V_{EE}}{R_E} \\ &= \frac{-1.32 - 0.75 + 5.2}{0.779} \\ &\simeq 4 \text{ mA} \end{aligned}$$

(If we wish, we can iterate to determine a better estimate of $V_{BE}|_{Q_R}$ and hence of I_E.) Assuming that Q_R has a high β so that its $\alpha \simeq 1$, its collector current will be approximately 4 mA. If we neglect the base current of Q_2, we obtain for the collector voltage of Q_R

$$V_C|_{Q_R} \simeq -4 \times 0.245 = -0.98 \text{ V}$$

Thus a first approximation for the value of the output voltage V_{OL} is

$$\begin{aligned} V_{OL} &= V_C|_{Q_R} - V_{BE}|_{Q_2} \\ &\simeq -0.98 - 0.75 = -1.73V \end{aligned}$$

We can use this value to find the emitter current of Q_2 and then iterate to determine a better estimate of its base–emitter voltage. The result is $V_{BE2} \simeq 0.79$ V and, correspondingly,

$$V_{OL} \simeq -1.77 \text{ V}$$

At this value of output voltage, Q_2 supplies a load current of about 4.6 mA.

To find the value of V_{OH} we assume that Q_R is completely cut off (because $v_I > V_{IH}$). Thus the circuit for determining V_{OH} simplifies to that in Fig. x8.27. Analysis of this circuit, assuming $\beta_2 = 100$, results in $V_{BE2} \simeq 0.83$ V, $I_{E2} = 22.4$ mA, and

$$V_{OH} \simeq -0.88 \text{ V}$$

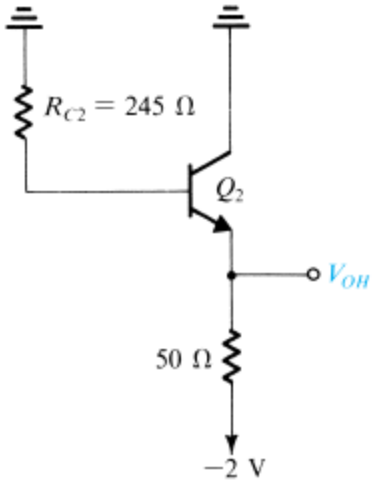

Figure x8.27 Circuit for determining V_{OH}.

EXERCISE

x8.17 For the circuit in Fig. x8.25, determine the values of I_E obtained when $v_I = V_{IL}$, V_R, and V_{IH}. Also, find the value of v_{OR} corresponding to $v_I = V_R$. Assume that $v_{BE} = 0.75$ V at a current of 1 mA.

Ans. 3.97 mA; 4.00 mA; 4.12 mA; –1.31 V

Noise Margins The results of Exercise x8.17 indicate that the bias current I_E remains approximately constant. Also, the output voltage corresponding to $v_I = V_R$ is approximately equal to V_R. Notice further that this is also approximately the midpoint of the logic swing; specifically,

$$\frac{V_{OL} + V_{OH}}{2} = -1.325 \simeq V_R$$

Thus the output logic levels are centered around the midpoint of the input transition band. This is an ideal situation from the point of view of noise margins, and it is one of the reasons for selecting the rather arbitrary-looking numbers ($V_R = -1.32$ V and $V_{EE} = 5.2$ V) for reference and supply voltages.

The noise margins can now be evaluated as follows:

$$NM_H = V_{OH} - V_{IH} = -0.88 - (-1.205) = 0.325 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = -1.435 - (-1.77) = 0.335 \text{ V}$$

Note that these values are approximately equal.

The NOR Transfer Curve The NOR transfer characteristic, which is v_{NOR} versus v_I for the circuit in Fig. x8.25, is sketched in Fig. x8.28. The values of V_{IL} and V_{IH} are identical to those found earlier for the OR characteristic. To emphasize this, we have labeled the threshold points x and y, the same letters used in Fig. x8.26.

For $v_I < V_{IL}$, Q_A is off and the output voltage v_{NOR} can be found by analyzing the circuit composed of R_{C1}, Q_3, and its 50-Ω termination. Except that R_{C1} is slightly smaller than R_{C2}, this circuit is identical to that in Fig. x8.27. Thus the output voltage will be only slightly greater than the value V_{OH} found earlier. In the sketch of Fig. x8.28 we have assumed that the output voltage is approximately equal to V_{OH}.

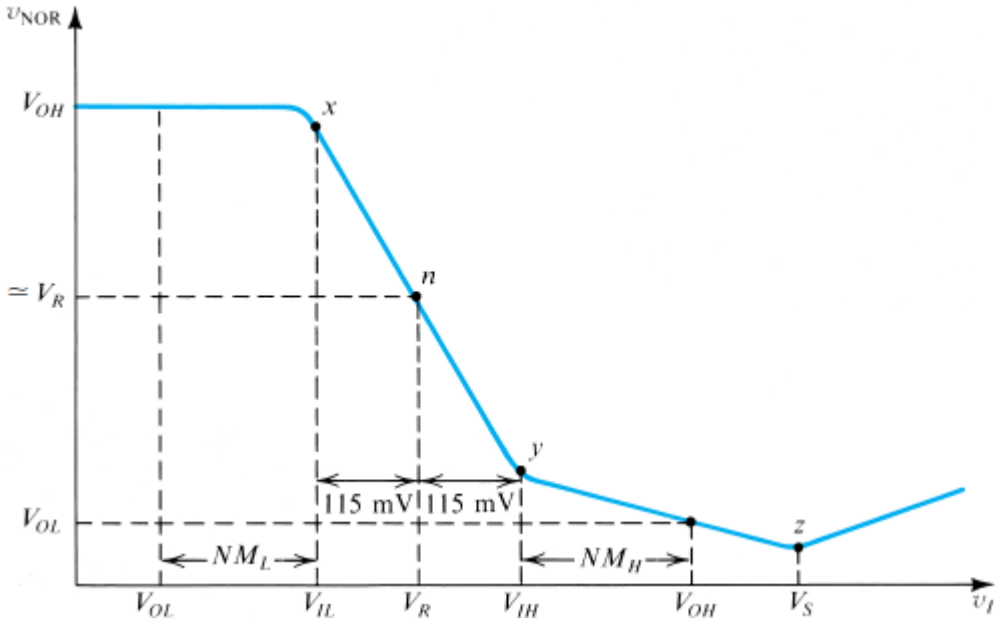

Figure x8.28 The NOR transfer characteristic, v_{NOR} versus v_I, for the circuit in Fig. x8.25.

For $v_I > V_{IH}$, Q_A is on and is conducting the entire bias current. The circuit then simplifies to that in Fig. x8.29. This circuit can be easily analyzed to obtain v_{NOR} versus v_I for the range $v_I \geq V_{IH}$. A number of observations are in order. First, note that $v_I = V_{IH}$ results in an output voltage slightly higher than V_{OL}. This is because R_{C1} is smaller than R_{C2}. In fact, R_{C1} is chosen lower in value than R_{C2} so that with v_I equal to the normal logic-1 value (i.e., V_{OH}, which is approximately –0.88 V), the output will be equal to the V_{OL} value found earlier for the OR output.

Second, note that as v_I exceeds V_{IH}, transistor Q_A operates in the active mode and the circuit of Fig. x8.29 can be analyzed to find the gain of this amplifier, which is the slope of the segment *yz* of the transfer characteristic. At point *z*, transistor Q_A saturates. Further increments in v_I (beyond the point $v_I = V_S$) cause the collector voltage and hence v_{NOR} to increase. The slope of the segment of the transfer characteristic beyond point *z*, however, is not unity, but is about 0.5, because as Q_A is driven deeper into saturation, a portion of the increment in v_I appears as an increment in the base–collector forward-bias voltage. The reader is urged to solve Exercise x8.18, which is concerned with the details of the NOR transfer characteristic.

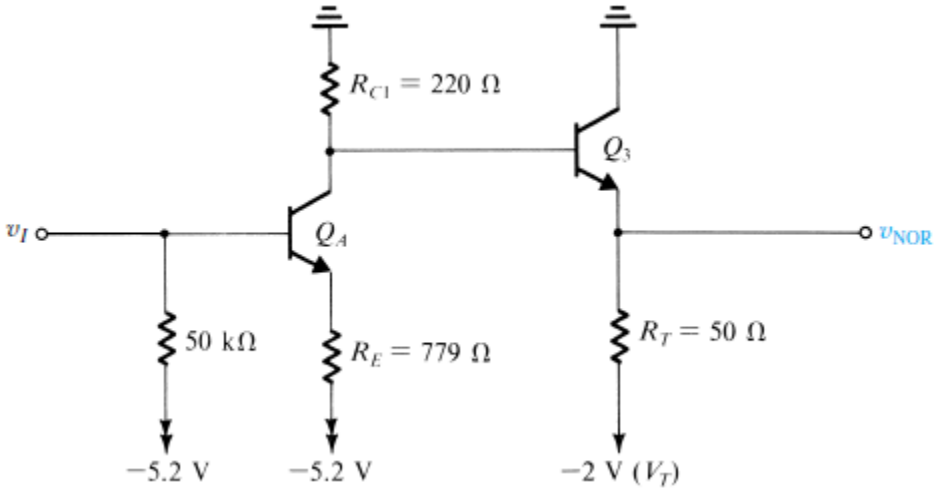

Figure x8.29 Circuit for finding v_{NOR} versus v_I for the range $V_I > V_{IH}$.

EXERCISE

x8.18 Consider the circuit in Fig. x8.29. (a) For $v_I = V_{IH} = -1.205$ V, find v_{NOR}. (b) For $v_I = V_{OH} = -0.88$ V, find v_{NOR}. (c) Find the slope of the transfer characteristic at the point $v_I = V_{OH} = -0.88$ V. (d) Find the value of v_I at which Q_A saturates (i.e., V_S). Assume that $V_{BE} = 0.75$V at a current of 1 mA, $V_{CEsat} \simeq 0.3$ V, and $\beta = 100$.

Ans. (a) –1.70 V; (b) –1.79 V; (c) –0.24 V/V; (d) –0.58 V

Manufacturers' Specifications ECL manufacturers supply gate transfer characteristics of the form shown in Figs. x8.26 and x8.28. A manufacturer usually provides such curves measured at a number of temperatures. In addition, at each relevant temperature, worst-case values for the parameters V_{IL}, V_{IH}, V_{OL}, and V_{OH} are given. These worst-case values are specified with the inevitable component tolerances taken into account. As an example, Motorola specifies that for MECL 10,000 at 25°C, the following worst-case values apply

$$V_{IL\max} = -1.475 \text{ V} \qquad V_{IH\min} = -1.105 \text{ V}$$
$$V_{OL\max} = -1.630 \text{ V} \qquad V_{OH\min} = -0.980 \text{ V}$$

These values can be used to determine words-case noise margins.

$$NM_L = 0.155 \text{ V} \qquad NM_H = 0.125 \text{ V}$$

which are about half the typical values previously calculated.

For additional information on MECL specifications the interested reader is referred to the Motorola (1988, 1989) publications listed in the bibliography in Appendix I.

x8.4.5 Fan-Out

When the input signal to an ECL gate is low (V_{OL}), the input current is equal to the current that flows in the 50-kΩ pull-down resistor. Thus,

$$I_{IL} = \frac{-1.77 + 5.2}{50} \simeq 69 \text{ μA}$$

When the input is high (V_{OH}), the input current is greater because of the base current of the input transistor. Thus, assuming a transistor β of 100, we obtain

$$I_{IH} = \frac{-0.88 + 5.2}{50} + \frac{4}{101} \simeq 126 \text{ μA}$$

Both these current values are quite small, which, coupled with the very small output resistance of the ECL gate, ensures that little degradation of logic-signal levels results from the input currents of fan-out gates. It follows that the fan-out of ECL gates is not limited by logic-level considerations but rather by the degradation of the circuit speed (rise and fall times). This latter effect is due to the capacitance that each fan-out gate presents to the driving gate (approximately 3 pF). Thus while the *dc fan-out* can be as high as 90 and thus does not represent a design problem, the *ac fan-out* is limited by considerations of circuit speed to 10 or so.

x8.4.6 Speed of Operation and Signal Transmission

The speed of operation of a logic family is measured by the delay of its basic gate and by the rise and fall times of the output waveforms. Typical values of these parameters for ECL have already been given. Here we should note that because the output circuit is an emitter follower, the rise time of the output signal is shorter than its fall time, since on the rising edge of the output pulse, the emitter follower functions and provides the output current required to charge up the load and parasitic capacitances. On the other hand, as

the signal at the base of the emitter follower falls, the emitter follower cuts off, and the load capacitance discharges through the combination of load and pull-down resistances.

To take full advantage of the very high speed of operation possible with ECL, special attention should be paid to the method of interconnecting the various logic gates in a system. To appreciate this point, we shall briefly discuss the problem of signal transmission.

ECL deals with signals whose rise times may be 1 ns or even less, the time it takes for light to travel only 30 cm or so. For such signals, a wire and its environment become a relatively complex circuit element along which signals propagate with finite speed (perhaps half the speed of light—i.e., 15 cm/ns). Unless special care is taken, energy that reaches the end of such a wire is not absorbed but rather returns as a *reflection* to the transmitting end, where (without special care) it may be re-reflected. The result of this process of reflection is what can be observed as **ringing**, a damped oscillatory excursion of the signal about its final value.

Unfortunately, ECL is particularly sensitive to ringing because the signal levels are so small. Thus it is important that transmission of signals be well controlled, and surplus energy absorbed, to prevent reflections. The accepted technique is to limit the nature of connecting wires in some way. One way is to insist that they be very short, where "short" is taken to mean with respect to the signal rise time. The reason for this is that if the wire connection is so short that reflections return while the input is still rising, the result becomes only a somewhat slowed and "bumpy" rising edge.

If, however, the reflection returns *after* the rising edge, it produces not simply a modification of the initiating edge but an *independent second event.* This is clearly bad! Thus the time taken for a signal to go from one end of a line and back is restricted to less than the rise time of the driving signal by some factor—say, 5. Thus for a signal with a 1-ns rise time and for propagation at the speed of light (30 cm/ns), a double path of only 0.2-ns equivalent length, or 6 cm, would be allowed, representing in the limit a wire only 3 cm from end to end.

Such is the restriction on ECL 100K. However, ECL 10K has an intentionally slower rise time of about 3.5 ns. Using the same rules, wires can accordingly be as long as about 10 cm for ECL 10K.

If greater lengths are needed, then transmission lines must be used. These are simply wires in a controlled environment in which the distance to a ground reference plane or a second wire is highly controlled. Thus they might simply be twisted pairs of wires, one of which is grounded, or parallel ribbon wires, every second of which is grounded, or so-called microstrip lines on a printed-circuit board. The latter are simply copper strips of controlled geometry on one side of a thin printed-circuit board, the other side of which consists of a grounded plane.

Such transmission lines have a *characteristic impedance*, R_0, that ranges from a few tens of ohms to hundreds of ohms. Signals propagate on such lines somewhat more slowly than the speed of light, perhaps half as fast. When a transmission line is terminated at its receiving end in a resistance equal to its characteristic impedance, R_0, all the energy sent on the line is absorbed at the receiving end, and no reflections occur (since the termination acts as a limitless length of transmission line). Thus, signal integrity is maintained. Such transmission lines are said to be *properly terminated.* A properly terminated line appears at its sending end as a resistor of value R_0. The followers of ECL 10K with their open emitters and low output resistances (specified to be 7 Ω maximum) are ideally suited for driving transmission lines. ECL is also good as a line receiver. The simple gate with its high (50-kΩ) pull-down input resistor represents a very high resistance to the line. Thus a few such gates can be connected to a terminated line with little difficulty. Both these ideas are represented in Fig. x8.24.

x8.4.7 Power Dissipation

Because of the differential-amplifier nature of ECL, the gate current remains approximately constant and is simply steered from one side of the gate to the other depending on the input logic signals. Thus, the supply current and hence the gate power dissipation of unterminated ECL remain relatively constant independent of the logic state of the gate. It follows that no voltage spikes are introduced on the supply line. Such spikes can be a dangerous source of noise in a digital system. It follows that in ECL the need for supply-line bypassing[7] is not as great as in, say, TTL. This is another advantage of ECL.

At this juncture we should reiterate a point we made earlier, namely, that although an ECL gate would operate with $V_{EE} = 0$ and $V_{CC} = +5.2$ V, the selection of $V_{EE} = -5.2$ V and $V_{CC} = 0$ V is recommended, because in the circuit, all signal levels are referenced to V_{CC}, and ground is certainly an excellent reference.

EXERCISE

x8.19 For the ECL gate in Fig. x8.23, calculate an approximate value for the power dissipated in the circuit under the condition that all inputs are low and that the emitters of the output followers are left open. Assume that the reference circuit supplies four identical gates, and hence only a quarter of the power dissipated in the reference circuit should be attributed to a single gate.

Ans. 22.4 mW

x8.4.8 Thermal Effects

In our analysis of the ECL gate of Fig. x8.23, we found that at room temperature the reference voltage V_R is –1.32 V. We have also shown that the midpoint of the output logic swing is approximately equal to this voltage, which is an ideal situation in that it results in equal high and low noise margins. In Example x8.2, we shall derive expressions for the temperature coefficients of the reference voltage and of the output low and high voltages. In this way, it will be shown that the midpoint of the output logic swing varies with temperature at the same rate as the reference voltage. As a result, although the magnitudes of the high and low noise margins change with temperature, their values remain equal. This is an added advantage of ECL and provides a demonstration of the high degree of design optimization of this gate circuit.

Example x8.2

We wish to determine the temperature coefficient of the reference voltage VR and of the midpoint between V_{OL} and V_{OH}.

Solution

To determine the temperature coefficient of V_R, consider the circuit in Fig. xE8.15 and assume that the temperature changes by +1°C. Denoting the temperature coefficient of the diode and transistor

voltage drops by δ, where $\delta \simeq -2$ mV/°C, we obtain the equivalent circuit shown in Fig. x8.30. In the latter circuit, the changes in device voltage drops are considered as signals, and hence the power supply is shown as a signal ground.

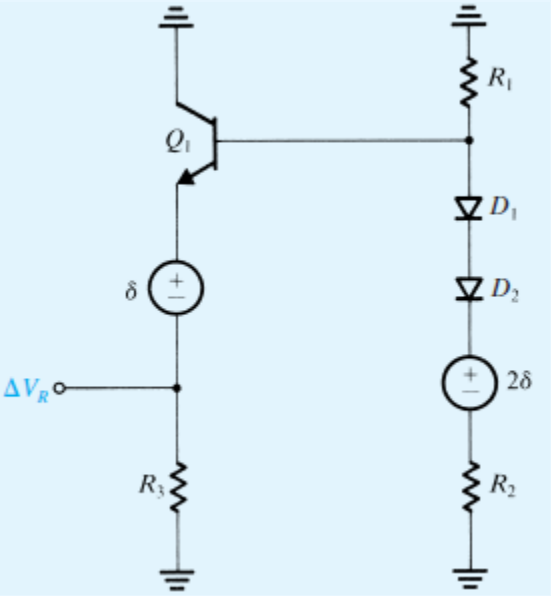

Figure x8.30 Equivalent circuit for determining the temperature coefficient of the reference voltage V_R.

In the circuit of Fig. x8.30 we have two signal generators, and we wish to analyze the circuit to determine ΔV_R, the change in V_R. We shall do so using the principle of superposition.[8] Consider first the branch R_1, D_1, D_2, 2 δ, and R_2, and neglect the signal base current of Q_1. The voltage signal at the base of Q_1 can be easily obtained from

$$v_{b1} = \frac{2\delta \times R_1}{R_1 + r_{d1} + r_{d2} + R_2}$$

where r_{d1} and r_{d2} denote the incremental resistances of diodes D_1 and D_2, respectively. The dc bias current through D1 and D2 is approximately 0.64 mA, and thus $r_{d1} = r_{d2} = 39.5\ \Omega$. Hence $v_{b1} \simeq 0.3\delta$. Since the gain of the emitter follower Q_1 is approximately unity, it follows that the component of ΔV_R due to the generator 2δ is approximately equal to v_{b1}, that is, $\Delta V_{R1} = 0.3\delta$.

Consider next the component of ΔV_R due to the generator δ. Reflection into the emitter circuit of the total resistance of the base circuit, $[R_1 \parallel (r_{d1} + r_{d2} + R_2)]$, by dividing it by $\beta + 1$ (with $\beta \simeq 100$) results in the following component of ΔV_R:

$$\Delta V_{R2} = -\frac{\delta \times R_3}{[R_B/(\beta + 1)] + r_{e1} + R_3}$$

Here R_B denotes the total resistance in the base circuit, and re1 denotes the emitter resistance of Q_1 ($\simeq 40\ \Omega$). This calculation yields $\Delta V_{R2} \simeq -\delta$. Adding this value to that due to the generator 2δ gives $\Delta V_R \simeq -0.7\delta$. Thus for $\delta = -2$ mV/°C the temperature coefficient of V_R is +1.4 mV/°C.

We next consider the determination of the temperature coefficient of V_{OL}. The circuit on which to perform this analysis is shown in Fig. x8.31. Here we have three generators whose contributions can be considered separately and the resulting components of ΔV_{OL} summed. The result is

$$\Delta V_{OL} = \Delta V_R \frac{-R_{C2}}{r_{eR} + R_E} \frac{R_T}{R_T + r_{e2}}$$
$$= -\delta \frac{-R_{C2}}{r_{eR} + R_E} \frac{R_T}{R_T + r_{e2}}$$
$$= -\delta \frac{R_T}{R_T + r_{e2} + R_{C2}/(\beta + 1)}$$

Substituting the values given and those obtained throughout the analysis of this section, we find

$$\Delta V_{OL} \simeq -0.43\delta$$

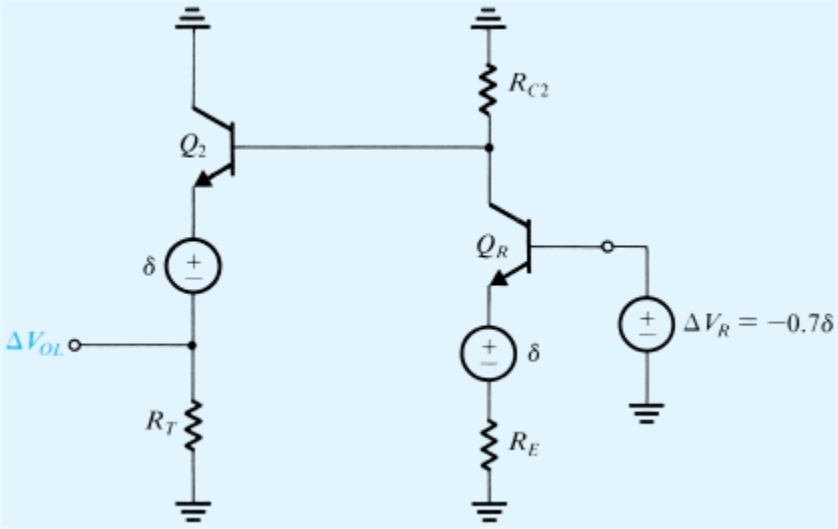

Figure x8.31 Equivalent circuit for determining the temperature coefficient of V_{OL}.

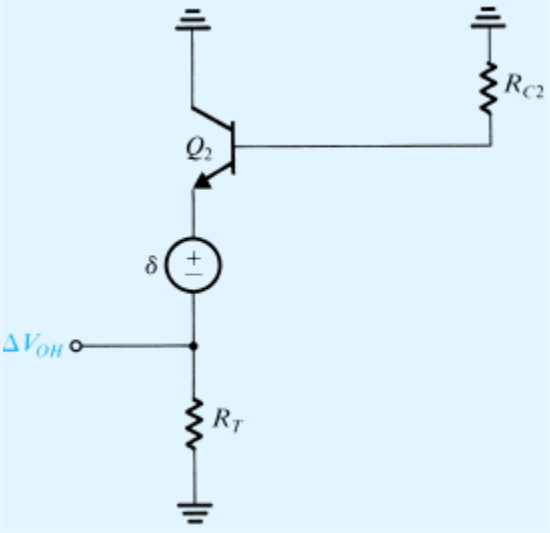

Figure x8.32 Equivalent circuit for determining the temperature coefficient of V_{OH}.

The circuit for determining the temperature coefficient of V_{OH} is shown in Fig. x8.32, from which we obtain

$$\Delta V_{OH} = -\delta \frac{R_T}{R_T + r_{e2} + R_{C2}/(\beta + 1)} = -0.93\delta$$

We now can obtain the variation of the midpoint of the logic swing as

$$\frac{\Delta V_{OL} + \Delta V_{OH}}{2} = -0.68\delta$$

which is approximately equal to that of the reference voltage $V_R(-0.7\delta)$.

x8.4.9 The Wired-OR Capability

The emitter–follower output stage of the ECL family allows an additional level of logic to be performed at very low cost by simply wiring the outputs of several gates in parallel. This is illustrated in Fig. x8.33, where the outputs of two gates are wired together. Note that the base–emitter diodes of the output followers realize an OR function: This **wired-OR** connection can be used to provide gates with high fan-in as well as to increase the flexibility of ECL in logic design.

x8.4.10 Final Remarks

We have chosen to study ECL by focusing on a commercially available circuit family. As we have shown, a great deal of design optimization has been applied to create a very-high-performance family of SSI and MSI logic circuits. ECL and some of its variants are also used in VLSI circuit design. Applications include very-high-speed processors such as those used in supercomputers, as well as high-speed and high-frequency communication systems. When used in VLSI design, current–source biasing is almost always utilized. Further, a variety of circuit configurations are used (see Rabaey, 1996).

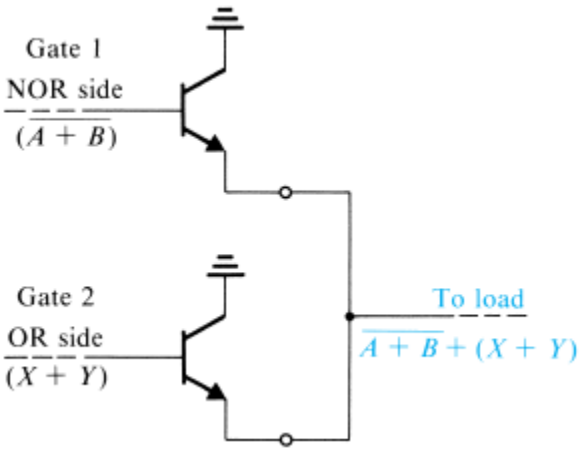

Figure x8.33 The wired-OR capability of ECL.

x8.5 BiCMOS Digital Circuits

In this section, we provide an introduction to a VLSI circuit technology that has at times been popular, BiCMOS. As its name implies, BiCMOS technology combines *bi*polar and *CMOS* circuits on one IC chip. The aim is to combine the low-power, high-input impedance and wide noise margins of CMOS with the high current-driving capability of bipolar transistors. Specifically, CMOS, although a nearly ideal logic-circuit technology in many respects, has a limited current-driving capability. This is not a serious problem when the CMOS gate has to drive a few other CMOS gates. It becomes a serious issue, however, when relatively large capacitive loads (e.g., greater than 0.5 pF or so) are present. In such cases, one has to either resort to the use of elaborate CMOS buffer circuits or face the usually unacceptable consequence of long propagation delays. On the other hand, we know that by virtue of its much larger transconductance, the BJT is capable of large output currents. We have seen a practical illustration of that in the emitter–follower output stage of ECL. Indeed, the high current-driving capability contributes to making ECL two to five times faster than CMOS (under equivalent conditions)—of course, at the expense of high power dissipation. In summary, then, BiCMOS seeks to combine the best of the CMOS and bipolar technologies to obtain a class of circuits that is particularly useful when output currents that are higher than possible with CMOS are needed. Furthermore, since BiCMOS technology is well suited for the implementation of high-performance analog circuits (see, e.g., Section x8.3), it makes possible the realization of both analog and digital functions on the same IC chip, making the "**system on a chip**" an attainable goal. The price paid is a more complex, and hence more expensive (than CMOS) processing technology.

x8.5.1 The BiCMOS Inverter

A variety of BiCMOS inverter circuits have been proposed and are in use. All of these are based on the use of *npn* transistors to increase the output current available from a CMOS inverter. This can be most simply achieved by cascading each of the Q_N and Q_P devices of the CMOS inverter with an *npn* transistor, as shown in Fig. x8.34(a). Observe that this circuit can be thought of as utilizing the pair of complementary composite MOS-BJT devices shown in Fig. x8.34(b). These composite devices retain the high input impedance of the MOS transistor while in effect multiplying its rather low g_m by the β of the BJT. It is also useful to observe that the output stage formed by Q_1 and Q_2 has what is known as the **totem-pole configuration** utilized by TTL.

The circuit of Fig. x8.34(a) operates as follows: When v_I is low, both Q_N and Q_2 are off while Q_P conducts and supplies Q_1 with base current, thus turning it on. Transistor Q_1then provides a large output current to charge the load capacitance. The result is a very fast charging of the load capacitance and correspondingly a short low-to-high propagation delay, t_{PLH} . Transistor Q_1 turns off when v_O reaches a value of about $V_{DD} - V_{BE1}$, and thus the output high level is lower than V_{DD}, a disadvantage. When v_I goes high, Q_P and Q_1 turn off, and Q_N turns on, providing its drain current into the base of Q_2. Transistor Q_2 then turns on and provides a large output current that quickly discharges the load capacitance. Here again the result is a short high-to-low propagation delay, t_{PHL}. On the negative side, Q_2 turns off when v_O reaches a value of about V_{BE2}, and thus the output low level is greater than zero, a disadvantage.

Thus, while the circuit of Fig. x8.34(a) features large output currents and short propagation delays, it has the disadvantage of reduced logic swing and, correspondingly, reduced noise margins. There is also another and perhaps more serious disadvantage, namely, the relatively long turn-off delays of Q_1 and Q_2 arising from the absence of

circuit paths along which the base charge can be removed. This problem can be solved by adding a resistor between the base of each of Q_1 and Q_2 and ground, as shown in Fig. x8.34(c). Now when either Q_1 or Q_2 is turned off, its stored base charge is removed to ground through R_1 or R_2, respectively. Resistor R_2 provides an additional benefit: With v_I

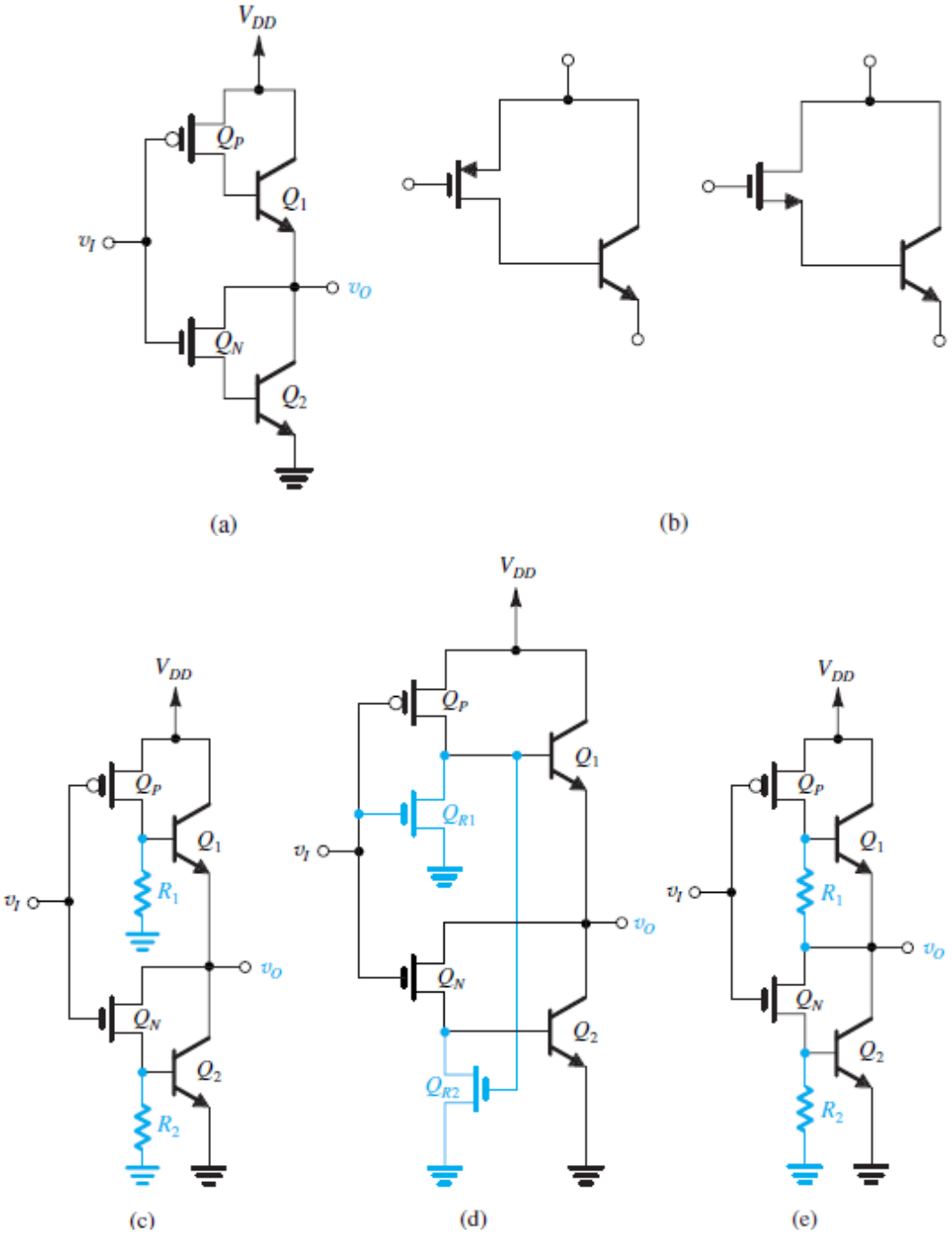

Figure x8.34 Development of the BiCMOS inverter circuit. **(a)** The basic concept is to use an additional bipolar transistor to increase the output current drive of each of Q_N and Q_P of the CMOS inverter. **(b)** The circuit in (a) can be thought of as utilizing these composite devices. **(c)** To reduce the turn-off times of Q_1 and Q_2, "bleeder resistors" R_1 and R_2 are added. **(d)** Implementation of the circuit in (c) using NMOS transistors to realize the resistors. **(e)** An improved version of the circuit in (c) obtained by connecting the lower end of R_1 to the output node.

high, and after Q_2 cuts off, v_O continues to fall below V_{BE2}, and the output node is pulled to ground through the series path of Q_N and R_2. Thus R_2 functions as a pull-down resistor. The Q_N–R_2 path, however, is a high-impedance one with the result that pulling v_O to ground is a rather slow process. Incorporating the resistor R_1, however, is disadvantageous from a static power-dissipation standpoint: When v_I is low, a dc path exists between V_{DD} and ground through the conducting Q_P and R_1. Finally, it should be noted that R_1 and R_2 take some of the drain currents of Q_P and Q_N away from the bases of Q_1 and Q_2 and thus slightly reduce the gate output current available to charge and discharge the load capacitance.

Figure x8.34(d) shows the way in which R_1 and R_2 are usually implemented. As indicated, NMOS devices Q_{R1} and Q_{R2} are used to realize R_1 and R_2. As an added innovation, these two transistors are made to conduct only when needed. Thus, Q_{R1} will conduct only when v_I rises, at which time its drain current constitutes a reverse base current for Q_1, speeding up its turn-off. Similarly, Q_{R2} will conduct only when v_I falls and Q_P conducts, pulling the gate of Q_{R2} high. The drain current of Q_{R2} then constitutes a reverse base current for Q_2, speeding up its turn-off.

As a final circuit for the BiCMOS inverter, we show the so-called *R*-circuit in Fig. x8.34(e). This circuit differs from that in Fig. x8.34(c) in only one respect: Rather than returning R_1 to ground, we have connected R_1 to the output node of the inverter. This simple change has two benefits. First, the problem of static power dissipation is now solved. Second, R_1 now functions as a pull-up resistor, pulling the output node voltage up to V_{DD} (through the conducting Q_P) after Q_1 has turned off. Thus, the *R* circuit in Fig. x8.34(e) does in fact have output levels very close to V_{DD} and ground.

As a final remark on the BiCMOS inverter, we note that the circuit is designed so that transistors Q_1 and Q_2 are never simultaneously conducting and neither is allowed to saturate. Unfortunately, sometimes the resistance of the collector region of the BJT in conjunction with large capacitive-charging currents causes saturation to occur. Specifically, at large output currents, the voltage developed across r_C (which can be of the order of 100 Ω) can lower the voltage at the intrinsic collector terminal and cause the CBJ to become forward biased. As the reader will recall, saturation is a harmful effect for two reasons: It limits the collector current to a value less than βI_B, and it slows down the transistor turn-off.

x8.5.2 Dynamic Operation

A detailed analysis of the dynamic operation of the BiCMOS inverter circuit is a rather complex undertaking. Nevertheless, an estimate of its propagation delay can be obtained by considering only the time required to charge and discharge a load capacitance *C*. Such an approximation is justified when *C* is relatively large and thus its effect on inverter dynamics is dominant: in other words, when we are able to neglect the time required to charge the parasitic capacitances present at internal circuit nodes. Fortunately, this is usually the case in practice, for if the load capacitance is not large, one would use the simpler CMOS inverter. In fact, it has been shown (Embabi, Bellaouar, and Elmasry, 1993) that the speed advantage of Bi-CMOS (over CMOS) becomes evident only when the gate is required to drive a large fan-out or a large load capacitance. For instance, at a load capacitance of 50 fF to 100 fF, BiCMOS and CMOS typically feature equal delays. However, at a load capacitance of 1 pF, t_P of a BiCMOS inverter is 0.3 ns, whereas that of an otherwise comparable CMOS inverter is about 1 ns.

Finally, in Fig. x8.35, we show simplified equivalent circuits that can be employed in obtaining rough estimates of t_{PLH} and t_{PHL} of the *R*-type BiCMOS inverter.

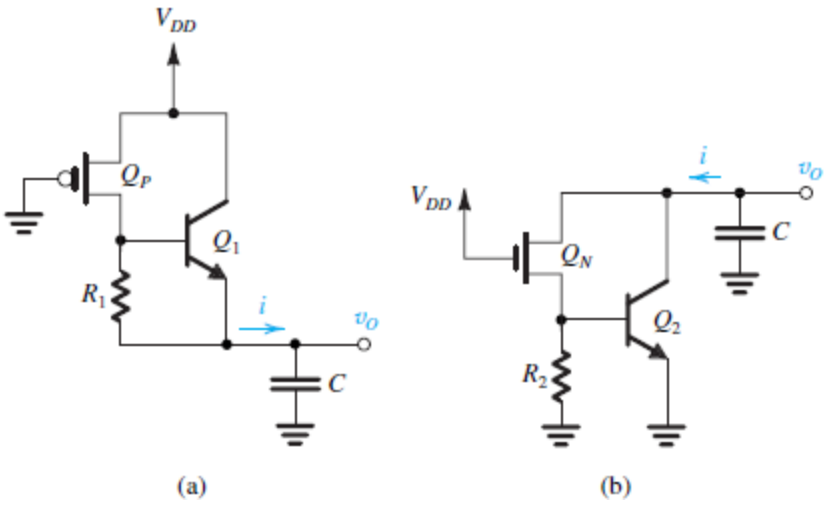

Figure x8.35 Equivalent circuits for charging and discharging a load capacitance *C*. Note that *C* includes all the capacitances present at the output node.

x8.5.3 BiCMOS Logic Gates

In BiCMOS, the logic is performed by the CMOS part of the gate, with the bipolar portion simply functioning as an output stage. It follows that BiCMOS logic-gate circuits can be generated following the same approach used in CMOS. As an example, we show in Fig. x8.36 a BiCMOS two-input NAND gate.

As a final remark, we note that BiCMOS technology is applied in a variety of products including microprocessors, static RAMs, and gate arrays (see Alvarez, 1993).

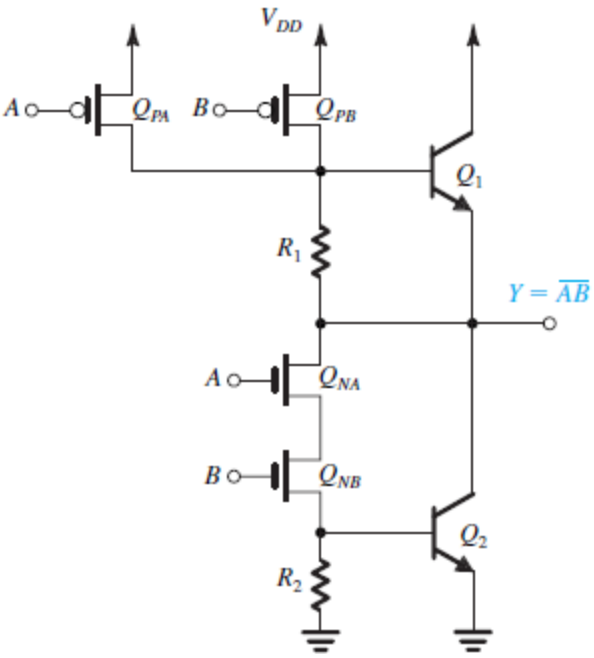

Figure x8.36 A BiCMOS two-input NAND gate.

EXERCISE

xD8.20 The threshold voltage of the BiCMOS inverter of Fig. x8.34(e) is the value of v_I at which both Q_N and Q_P are conducting equal currents and operating in the saturation region. At this value of v_I, Q_2 will be on, causing the voltage at the source of Q_N to be approximately 0.7 V. Design the circuit so that the threshold voltage is equal to $V_{DD}/2$. For $V_{DD} = 5$ V, $|V_t| = 0.6$ V, and assuming equal channel lengths for Q_N and Q_P and that $\mu_n \simeq 2.5\,\mu_p$, find the required ratio of widths, W_p / W_n.

Ans. 1