

# **Microelectronic Circuits**

## **8<sup>th</sup> Edition**

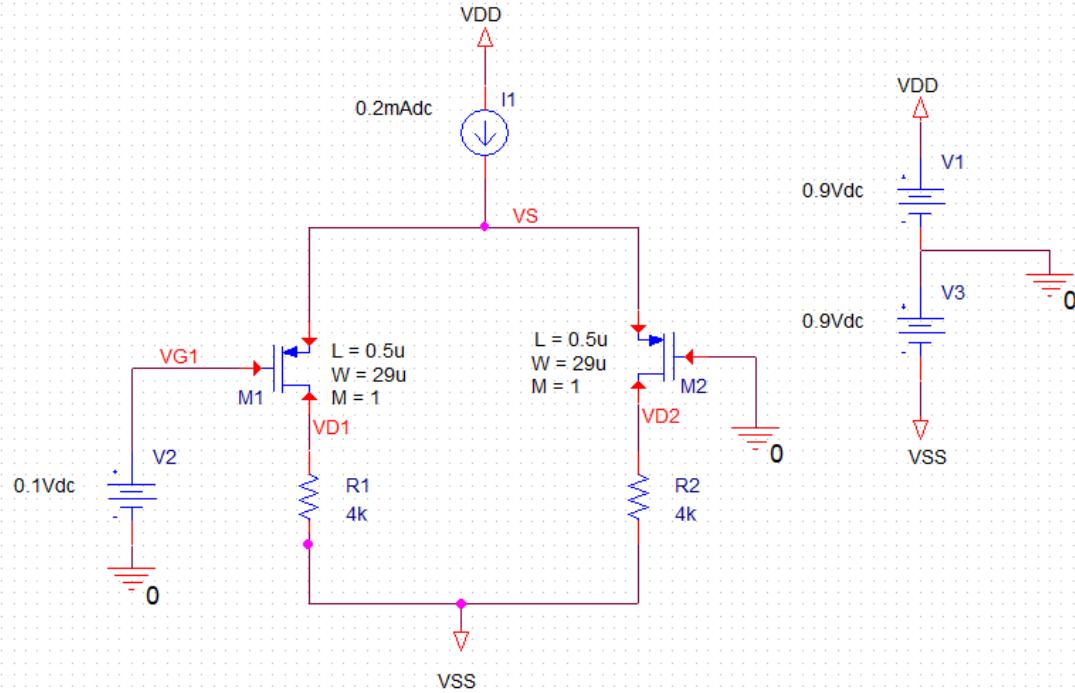
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*Spice Problems Solutions  
Chapter 9*

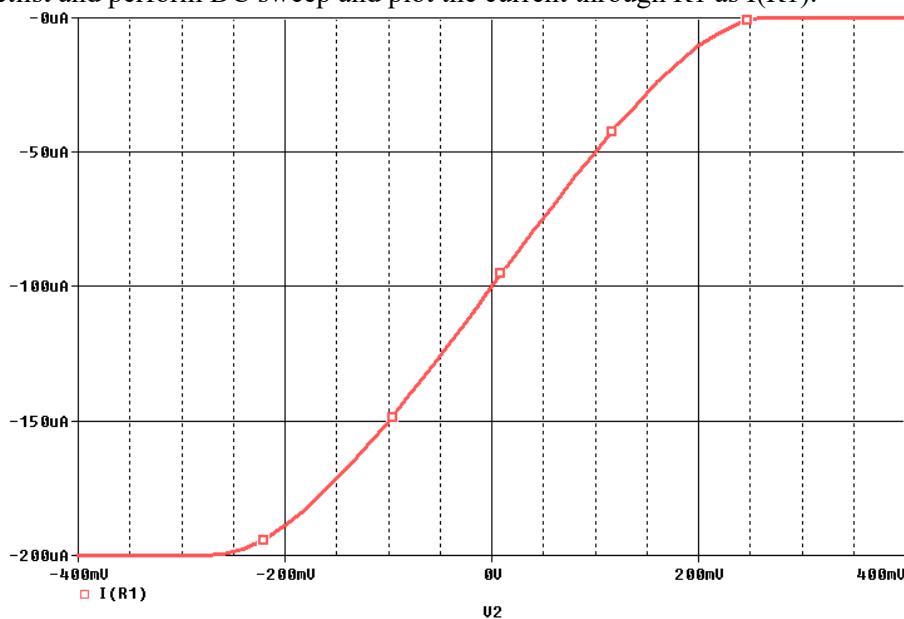
*Prepared by: Nijwm Wary  
2019*

**Problem: 9.4**

1. The schematic for this problem is shown below.



2. For the transistor model we have used,  $k'_p = 86 \mu\text{A}/\text{V}^2$ . So, the sizes for the transistors are  $\text{W}/\text{L} = 29\mu/0.5\mu$ .
3. Run the netlist and perform DC sweep and plot the current through R1 as  $I(R1)$ .



4. The current is completely steered from one branch to other when  $VG1(V2)=\pm 250$  mV.  
 5. When  $VG1(V2)=250$  mV, the voltages at the transistor drains and the common-source node are,

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( VS)	.6969	( VD1)	-.8972	( VD2)	-.1028	( VDD)	.9000
( VG1)	.2500	( VSS)	-.9000				

### Netlist:

Copy the netlist given below and paste it into a text file and save it with \*.cir extension.

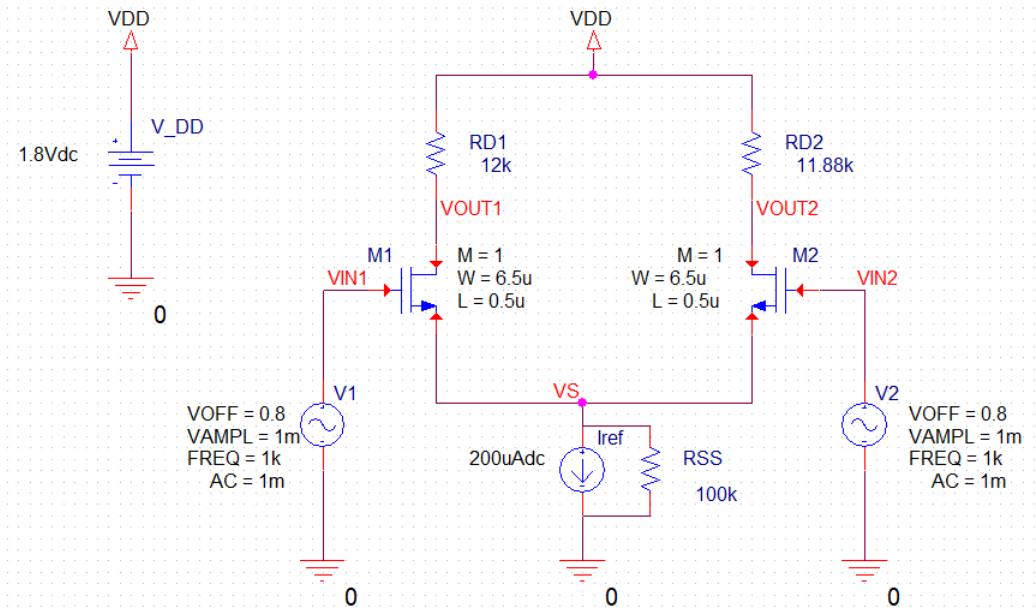
```
*****Problem: P9_4 ****
***** Main circuit begins here*****
M1      VD1 VG1 VS VDD PMOSOP18
+ L=0.5u
+ W=29u
+ M=1
M2      VD2 0 VS VDD PMOSOP18
+ L=0.5u
+ W=29u
+ M=1
R1      VSS VD1 4k TC=0,0
R2      VSS VD2 4k TC=0,0
I1      VDD VS DC 0.2mAdc
V1      VDD 0 0.9Vdc
V2      VG1 0 0.25Vdc
V3      0 VSS 0.9Vdc
***** Main circuit ends here*****


***** PMOS model (0.18um) begins here ****
.model PMOSOP18    PMOS(Level=1 VTO=-0.4 GAMMA=0.3 PHI=0.8
+ LD=0 WD=0 UO=102 LAMBDA=0.17 TOX=4.08E-9 PB=0.9 CJ=1E-3
+ CJSW=2.04E-10 MJ=0.45 MJSW=0.29 CGDO=3.43E-10 JS=4.0E-7 CGBO=3.5E-10
+ CGSO=3.43E-10)
***** PMOS model ends here *****

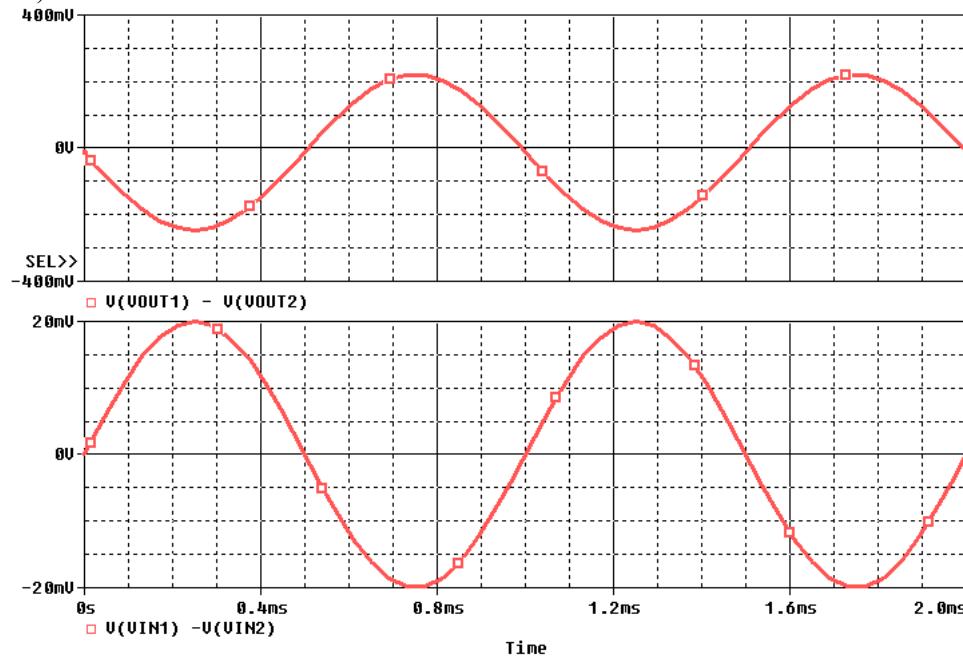
***** Analysis begins here*****
.OP
.DC [LIN] V2 -0.4 0.4 0.02
.PROBE
.END
***** Analysis ends here*****
```

**Problem: 9.55**

1. The schematic for this problem is shown below.



2. For the transistor model we have used,  $k'_n=380 \mu\text{A/V}^2$ . So, the sizes for the transistors are  $\text{W/L}=6.5\mu/0.5\mu$ .
3. Run the netlist and perform a transient analysis. Plot  $V(\text{VIN1})-V(\text{VIN2})$  and  $V(\text{VOUT1})-V(\text{VOUT2})$ .

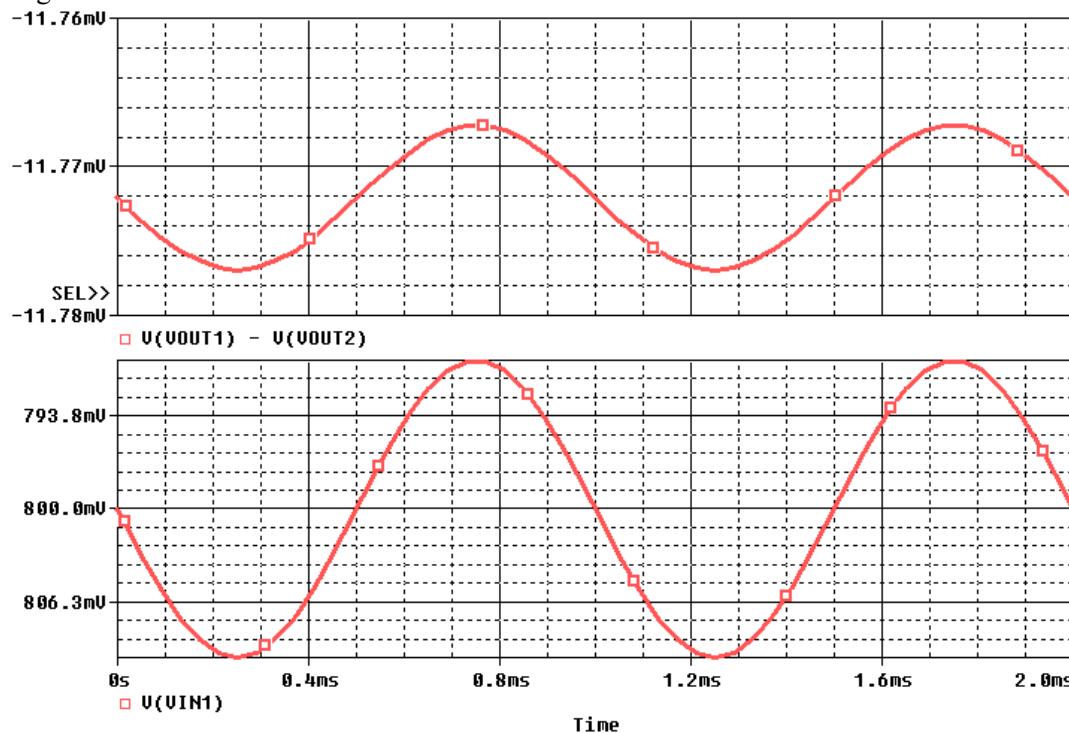


4. Using cursors, measure the differential gain of  $11.57 \text{ V/V}$ .

5. To simulate the common mode gain make the phase of V2 the same as that of V1 by changing the amplitude from -10m to 10m as follows

```
+SIN 0.8 10m 1k 0 0 0
```

6. Perform the transient analysis again and plot V(VIN1) and V(VOUT1). Calculate the common mode gain.



7. The common mode gain is  $4.85 \times 10^{-4}$  V/V.

8. Divide the two gains to get the CMRR.

### Netlist:

Copy the netlist given below and paste it into a text file and save it with \*.cir extension.

```
***** Problem: P9_55 *****
***** Main circuit begins here*****
V_DD      VDD 0 1.8Vdc
RD2       VOUT2 VDD 11.88k
Iref      VS 0 DC 200uAdc
RSS       0 VS 100k
RD1       VOUT1 VDD 12k
M1        VOUT1 VIN1 VS 0 NMOSOP18
+ L=0.5u
+ W=6.5u
+ M=1
M2        VOUT2 VIN2 VS 0 NMOSOP18
```

```

+ L=0.5u
+ W=6.5u
+ M=1
V1      VIN1 0  AC 1m
+SIN 0.8 10m 1k 0 0 0
V2      VIN2 0  AC 1m
+SIN 0.8 -10m 1k 0 0 0
***** Main circuit ends here*****  

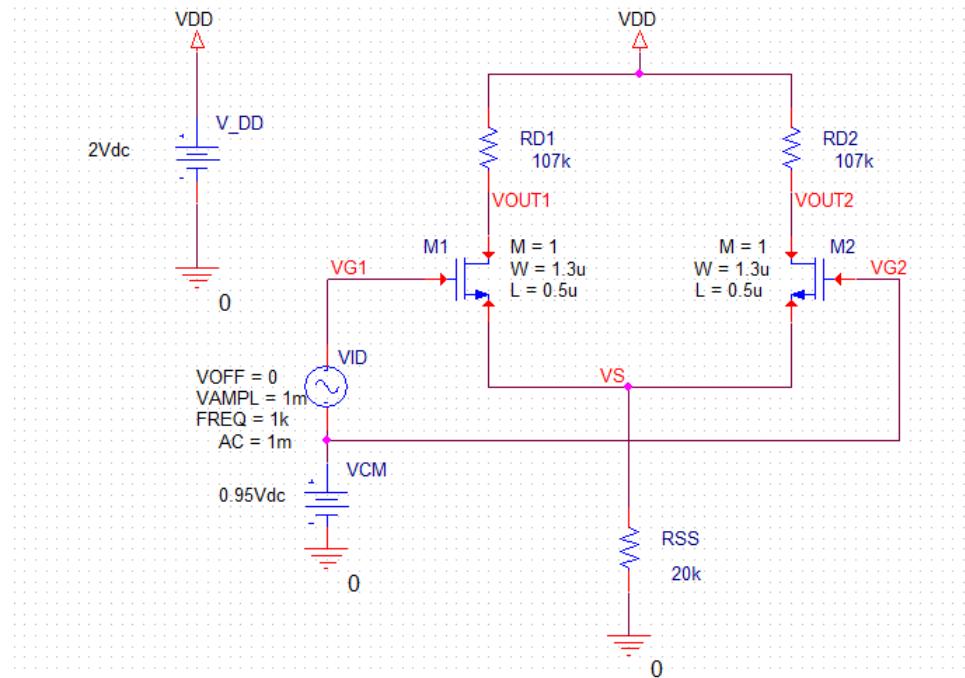
***** NMOS model begins here *****
.model NMOSOP18      NMOS(Level=1 VTO=0.5 GAMMA=0.3 PHI=0.84
+          LD=0 WD=0 UO=450 LAMBDA=0.02 TOX=4.08E-9 PB=0.9 CJ=1.6E-3
+          CJSW=2.04E-10 MJ=0.5 MJSW=0.2 CGDO=3.67E-10 JS=8.38E-6 CGBO=3.8E-10
+          CGSO=3.67E-10)
***** NMOS model ends here *****  

***** Analysis begins here*****
.TRAN 0.01mS 2mS
.PROBE
.END
***** Analysis ends here*****

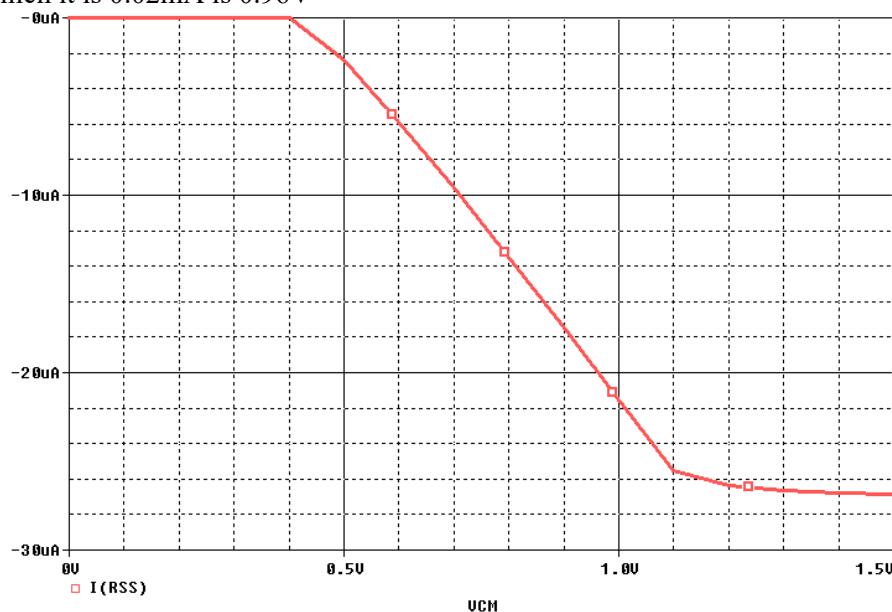
```

**Problem: 9.57**

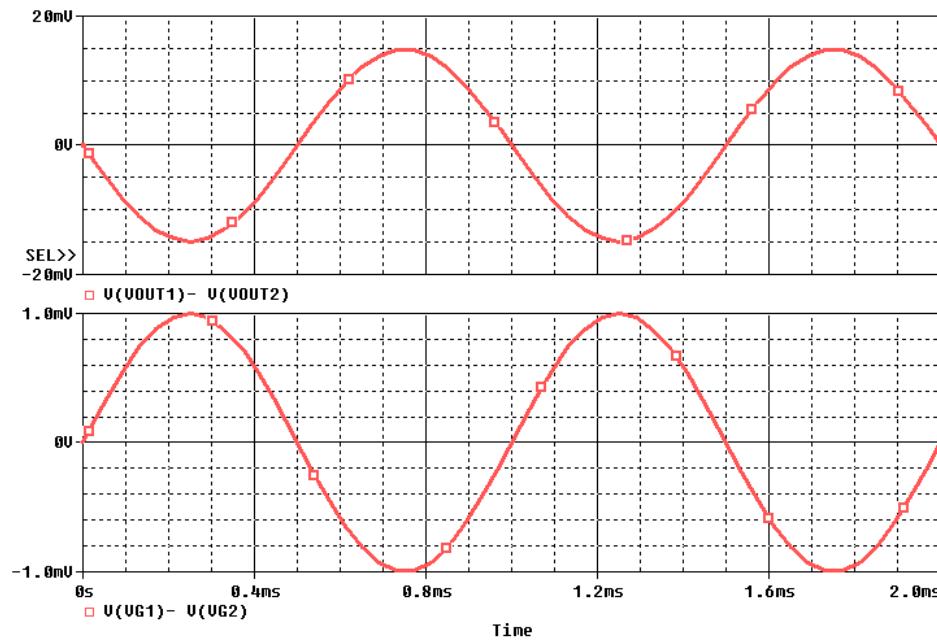
1. The schematic for this problem is shown below



2. For the transistor model that have been used,  $k'_n = 380 \mu\text{A/V}^2$ . So, the sizes for the transistors are taken as  $W/L = 1.3\mu/0.5\mu$ .
3. For part (a) run the netlist and perform DC sweep. Plot the current I(RSS) as shown below. The VCM at which it is 0.02mA is 0.96V



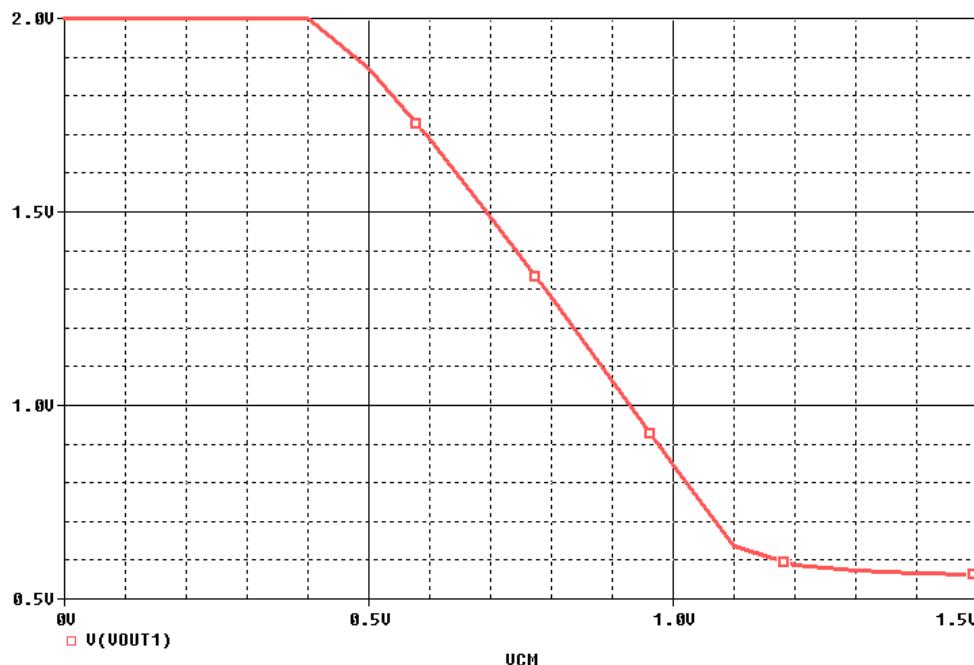
4. For part (b), uncomment the transient analysis statement and comment other analysis statements. Plot the input and output differential voltage. Find that for  $R_D=107\text{k}\Omega$ , the gain is 15 V/V as shown below.



5. For part (c), the drain voltages are,

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( VS )	.3903	( VDD )	2.0000	( VG1 )	.9500	( VG2 )	.9500
( VOUT1 )	.9558	( VOUT2 )	.9558				

6. For part (d) perform a DC sweep again as in part (a). Plot the voltage  $V(VOUT1)$  and find the slope to calculate the common-mode gain as shown below.



7. The common mode gain is -2.02 V/V.  
 8. The transistors enter the triode region when VCM=1.1V.

### Netlist:

Copy the netlist given below and paste it into a text file and save it with \*.cir extension.

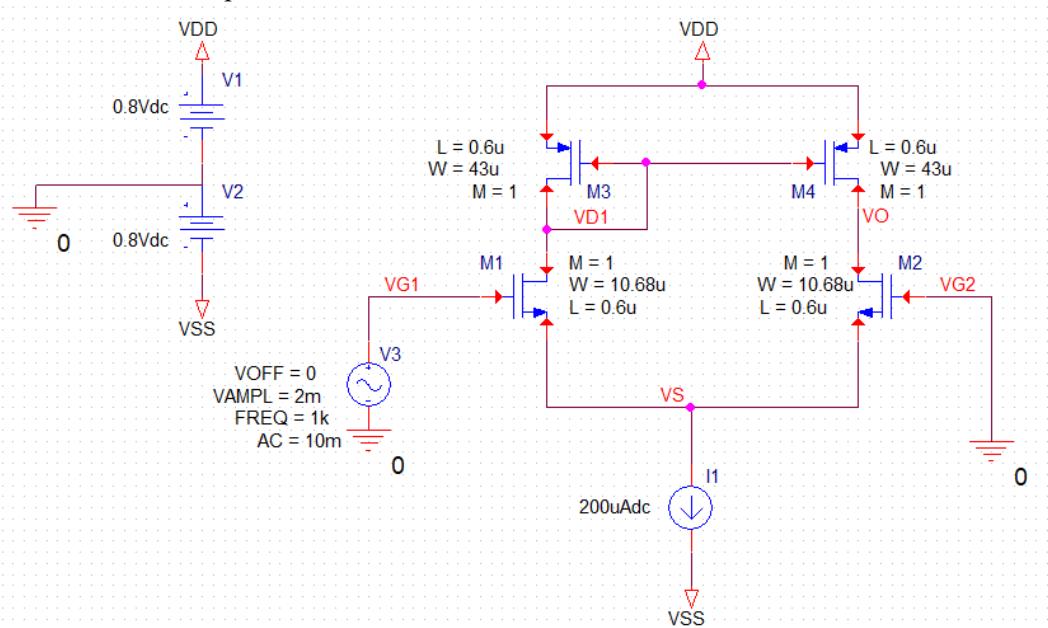
```
***** Problem: P9_57 *****
***** Main circuit begins here*****
V_DD      VDD 0 2Vdc
RD2       VOUT2 VDD 107k
RSS        0 VS 20k
RD1       VOUT1 VDD 107k
M1        VOUT1 VG1 VS 0 NMOSOP18
+ L=0.5u
+ W=1.3u
+ M=1
M2        VOUT2 VG2 VS 0 NMOSOP18
+ L=0.5u
+ W=1.3u
+ M=1
VID        VG1 VG2 AC 1m
+SIN 0 1m 1k 0 0 0
VCM        VG2 0 0.95Vdc
***** Main circuit ends here*****

***** NMOS model begins here *****
.model NMOSOP18   NMOS(Level=1 VTO=0.4 GAMMA=0.1 PHI=0.84
+ LD=0 WD=0 UO=450 LAMBDA=0.0 TOX=4.08E-9 PB=0.9 CJ=1.6E-3
+ CJSW=2.04E-10 MJ=0.5 MJSW=0.2 CGDO=3.67E-10 JS=8.38E-6 CGBO=3.8E-10
+ CGSO=3.67E-10
***** NMOS model ends here *****
```

```
***** Analysis begins here*****
.OP
.DC [LIN] VCM 0 1.5 0.1
*.TRAN 0.01mS 2mS
.PROBE
.END
***** Analysis ends here*****
```

**Problem: 9.99**

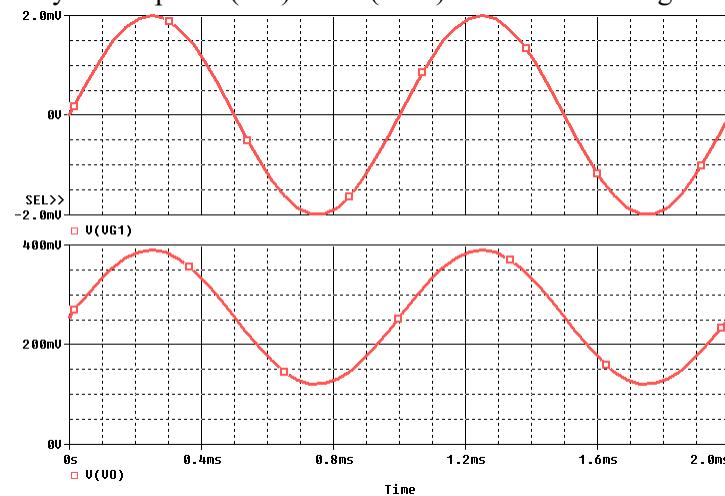
1. The schematic for this problem is shown below



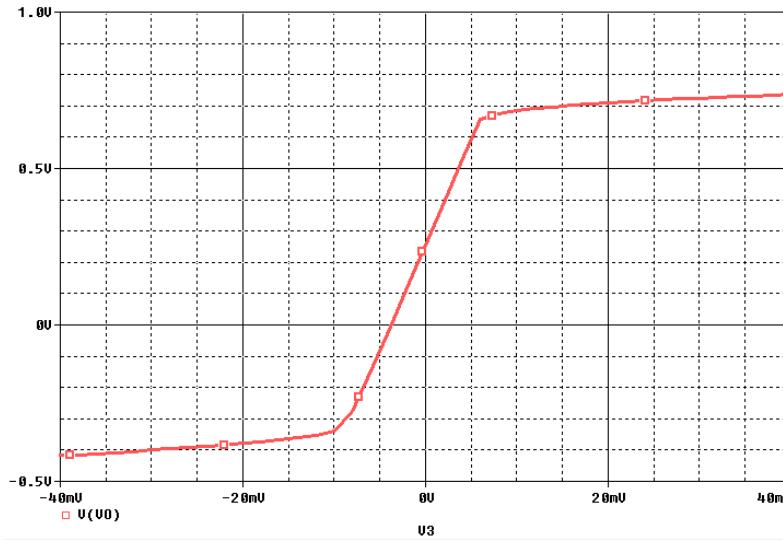
2. Perform the operating point analysis and see all the voltages and currents are as required by the problem statement.

NAME	M1	M2	M4	M3
MODEL	NMOS0P18	NMOS0P18	PMOS0P18	PMOS0P18
ID	9.93E-05	9.93E-05	-9.93E-05	-9.93E-05
VGS	4.67E-01	4.67E-01	-5.45E-01	-5.45E-01
VDS	7.22E-01	7.22E-01	-5.45E-01	-5.45E-01
VBS	4.67E-01	4.67E-01	0.00E+00	0.00E+00
VTH	3.24E-01	3.24E-01	-4.00E-01	-4.00E-01
VDSAT	1.44E-01	1.44E-01	-1.45E-01	-1.45E-01

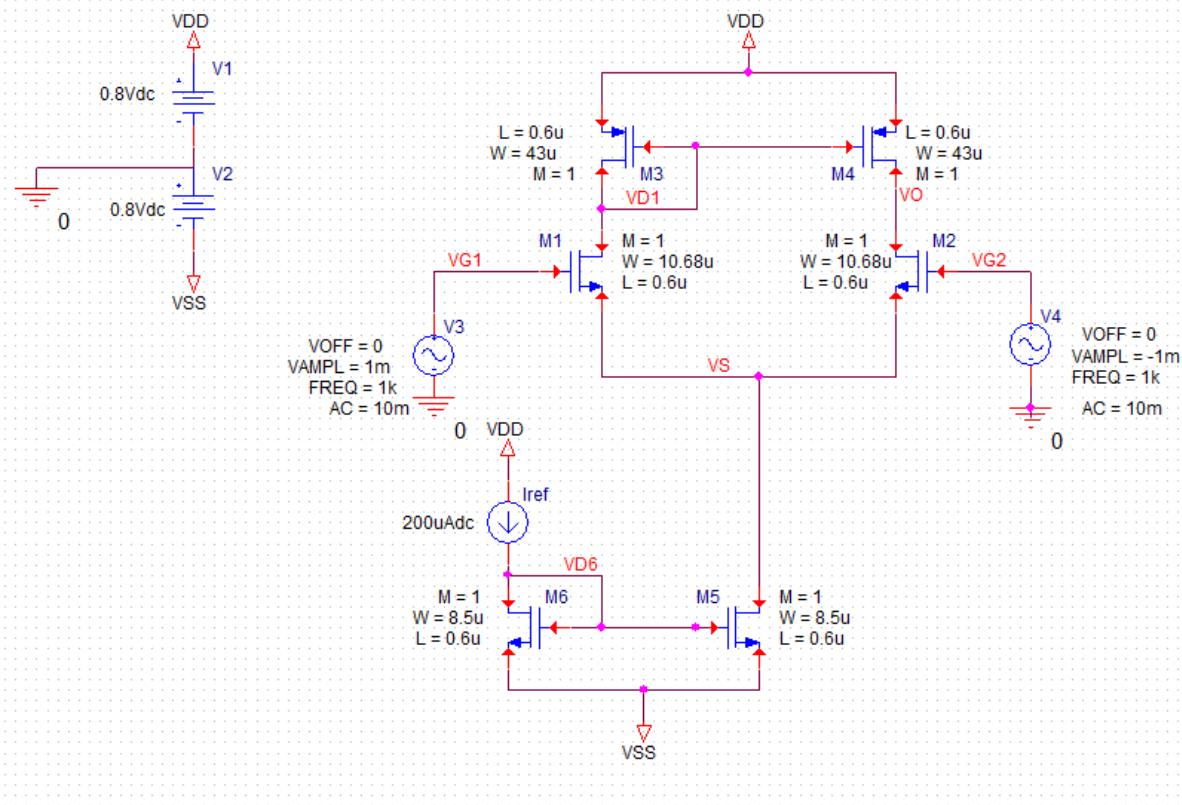
3. Run the transient analysis and plot  $V(VO)$  and  $V(VG1)$  and calculate the gain



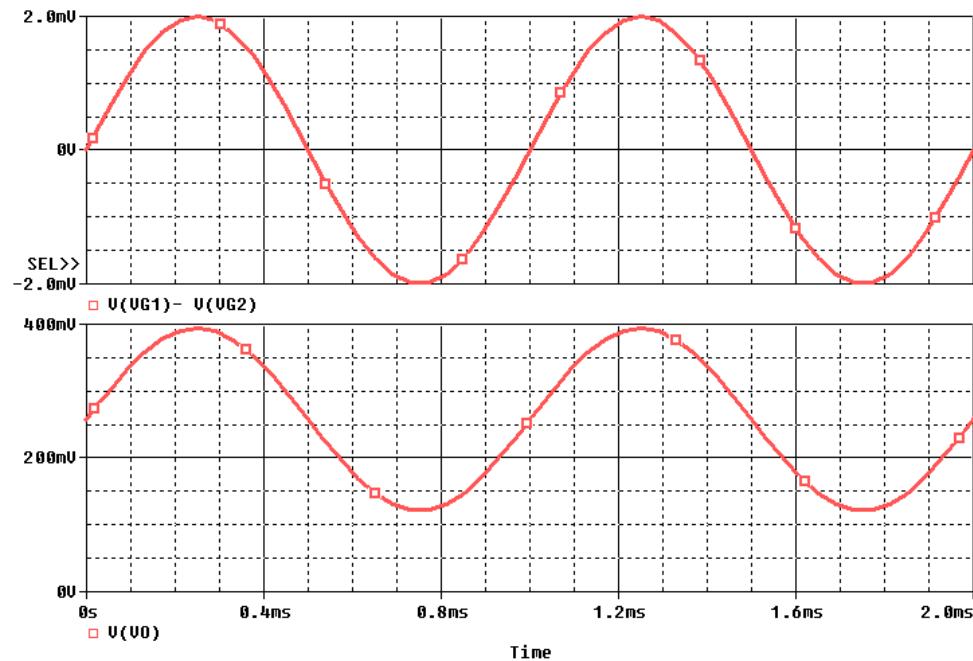
4. Perform DC sweep of the input voltage V3 and plot V(VO) to find its range by uncommenting this part of the analysis.



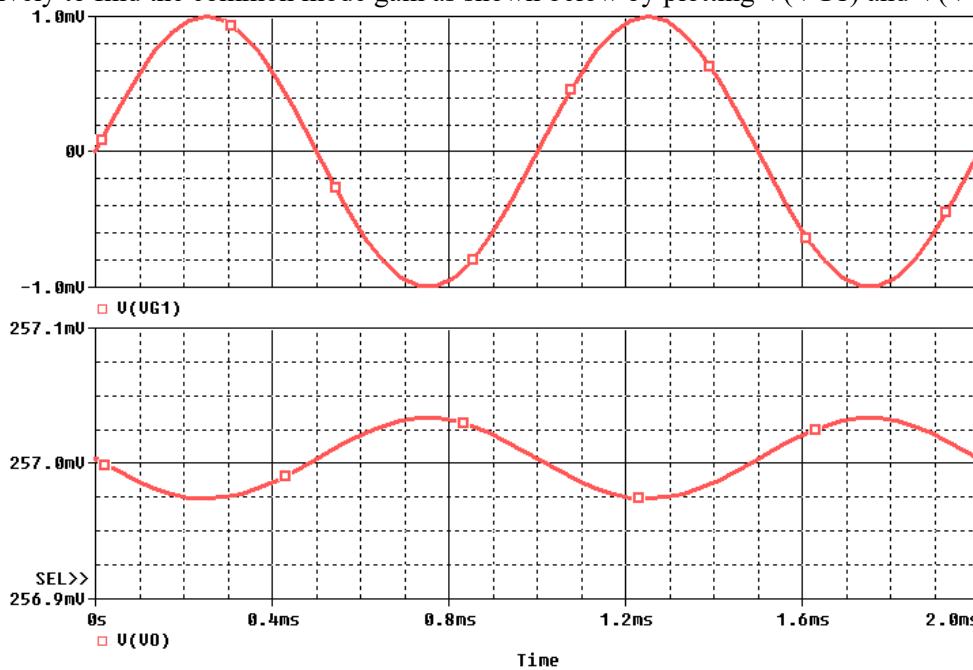
5. The allowable range of VO is from -0.33V to 0.67V.  
6. The schematic for part (d) is shown below.



7. Apply a voltage swing with amplitudes of 1 mV and -1 mV for the sources V3 and V4 respectively to find the differential gain as shown below by plotting  $V(VG1) - V(VG2)$  and  $V(VO)$ .



8. Apply a voltage swing with amplitudes of +1 mV and +1 mV for the sources V3 and V4 respectively to find the common mode gain as shown below by plotting  $V(VG1)$  and  $V(VO)$ .



9. The common mode gain is 0.03 V/V.

10. Divide the common mode gain by the differential gain to get the CMRR of 64.5 dB.

### **Netlist:**

For part (a), (b) and (c), copy the netlist given below and paste it into a text file and save it with \*.cir extension.

```
***** Problem: P9_99 (a), (b) and (c) *****
***** Main circuit begins here*****
M1      VD1 VG1 VS 0 NMOSOP18
+ L=0.6u
+ W=10.68u
+ M=1
M2      VO 0 VS 0 NMOSOP18
+ L=0.6u
+ W=10.68u
+ M=1
I1      VS VSS DC 200uAdc
M4      VO VD1 VDD VDD PMOSOP18
+ L=0.6u
+ W=42.66u
+ M=1
M3      VD1 VD1 VDD VDD PMOSOP18
+ L=0.6u
+ W=42.66u
+ M=1
V1      VDD 0 0.8Vdc
V2      0 VSS 0.8Vdc
V3      VG1 0 AC 10m
+SIN 0 2m 1k 0 0 0
***** Main circuit ends here*****

***** PMOS model begins here *****
.model PMOSOP18      PMOS(Level=1 VTO=-0.4 GAMMA=0.3 PHI=0.8
+ LD=0 WD=0 UO=148 LAMBDA=0.11 TOX=4.08E-9 PB=0.9 CJ=1E-3
+ CJSW=2.04E-10 MJ=0.45 MJSW=0.29 CGDO=3.43E-10 JS=4.0E-7 CGBO=3.5E-10
+ CGSO=3.43E-10)
***** PMOS model ends here *****

***** NMOS model begins here *****
.model NMOSOP18      NMOS(Level=1 VTO=0.4 GAMMA=0.3 PHI=0.84
+ LD=0 WD=0 UO=591 LAMBDA=0.11 TOX=4.08E-9 PB=0.9 CJ=1.6E-3
+ CJSW=2.04E-10 MJ=0.5 MJSW=0.11 CGDO=3.67E-10 JS=8.38E-6 CGBO=3.8E-10
+ CGSO=3.67E-10)
***** NMOS model ends here *****

***** Analysis begins here*****
.OP
.TRAN 0.01mS 2mS
*.DC [LIN] V3 -0.04 0.04 0.002
.PROBE
.END
***** Analysis ends here*****
```

For part (d), copy the netlist given below and paste it into a text file and save it with \*.cir extension.

```
***** Problem: P9_99 (d)*****
***** Main circuit begins here*****
V2      0 VSS 0.8Vdc
V1      VDD 0 0.8Vdc
M3      VD1 VD1 VDD VDD PMOSOP18
```

```

+ L=0.6u
+ W=43u
+ M=1
M2      VO VG2 VS 0 NMOSOP18
+ L=0.6u
+ W=10.68u
+ M=1
M4      VO VD1 VDD VDD PMOSOP18
+ L=0.6u
+ W=43u
+ M=1
M1      VD1 VG1 VS 0 NMOSOP18
+ L=0.6u
+ W=10.68u
+ M=1
V3      VG1 0 AC 10m
+SIN 0 1m 1k 0 0 0
Iref     VDD VD6 DC 200uAdc
M5      VS VD6 VSS 0 NMOSOP18
+ L=0.6u
+ W=8.5u
+ M=1
M6      VD6 VD6 VSS 0 NMOSOP18
+ L=0.6u
+ W=8.5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=1
V4      VG2 0 AC 10m
+SIN 0 -1m 1k 0 0 0
***** Main circuit ends here*****
```

```

***** PMOS model begins here *****
.model PMOSOP18    PMOS(Level=1 VTO=-0.4 GAMMA=0.3 PHI=0.8
+ LD=0 WD=0 UO=148 LAMBDA=0.11 TOX=4.08E-9 PB=0.9 CJ=1E-3
+ CJSW=2.04E-10 MJ=0.45 MJSW=0.29 CGDO=3.43E-10 JS=4.0E-7 CGBO=3.5E-10
+ CGSO=3.43E-10)
***** PMOS model ends here *****
```

```

***** NMOS model begins here *****
.model NMOSOP18    NMOS(Level=1 VTO=0.4 GAMMA=0.3 PHI=0.84
+ LD=0 WD=0 UO=591 LAMBDA=0.11 TOX=4.08E-9 PB=0.9 CJ=1.6E-3
+ CJSW=2.04E-10 MJ=0.5 MJSW=0.11 CGDO=3.67E-10 JS=8.38E-6 CGBO=3.8E-10
+ CGSO=3.67E-10)
***** NMOS model ends here *****
```

```

***** Analysis begins here*****
.OP
.TRAN 0.01mS 2mS
.PROBE
.END
***** Analysis ends here*****
```