Microelectronic Circuits
8th Edition

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Spice Examples for
Appendix B

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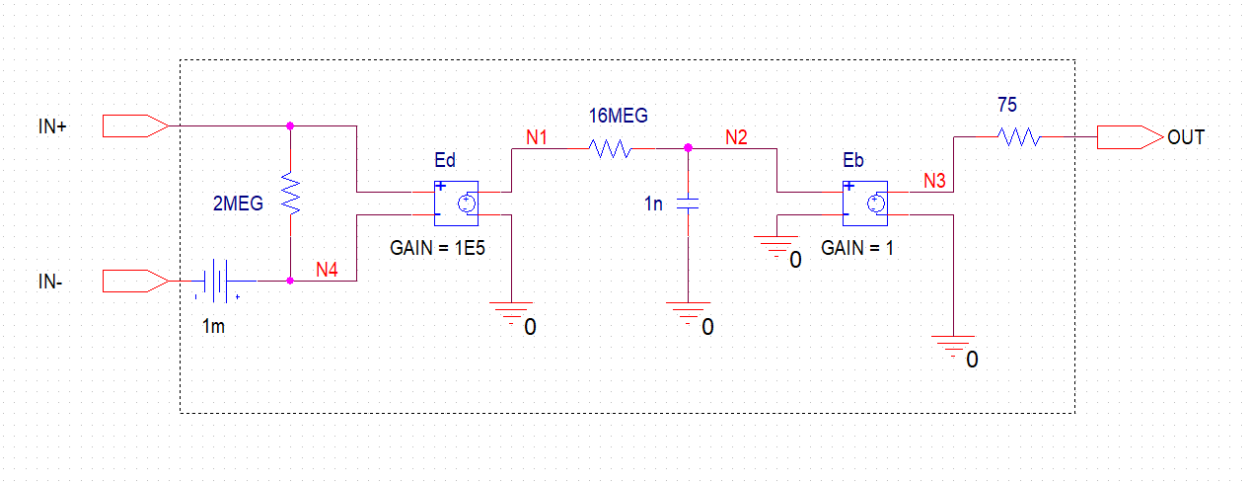
Example S.2.1

(a) The schematic for this example is shown below

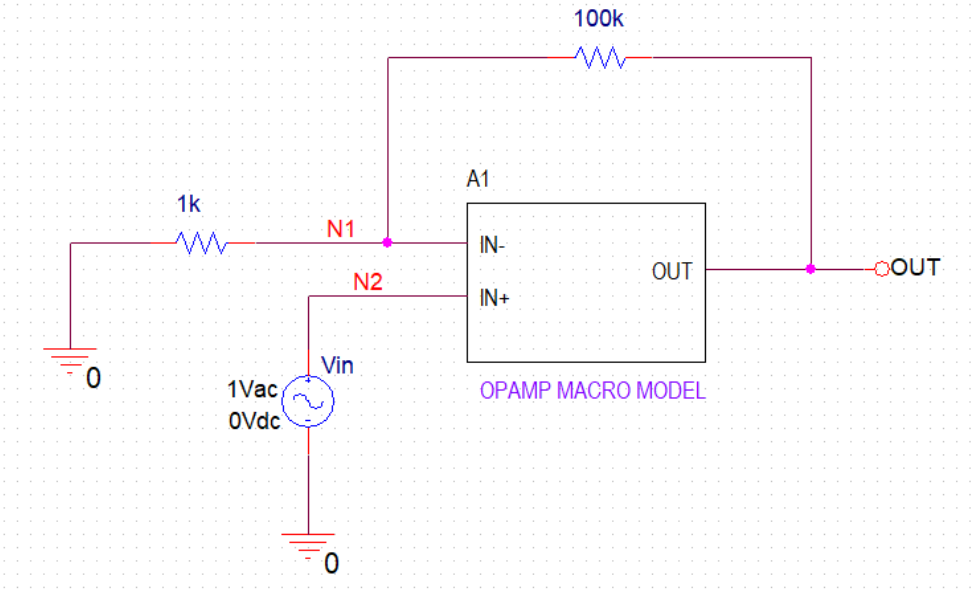


Netlist:

The netlist is given below

```
.SUBCKT OPAMP_MACRO    IN+ IN- OUT
Ro          OUT N3  75
VOS          N4 IN- 1m
Eb          N3 0 N2 0 1
Rb          N2 N1  16MEG
Cb          0 N2  1n
Ed          N1 0 IN+ N4 1E5
Rid          IN+ N4  2MEG
.ENDS
```

(b) The schematic for this part of the example, sub-parts (i), (ii) and (iii) is shown below

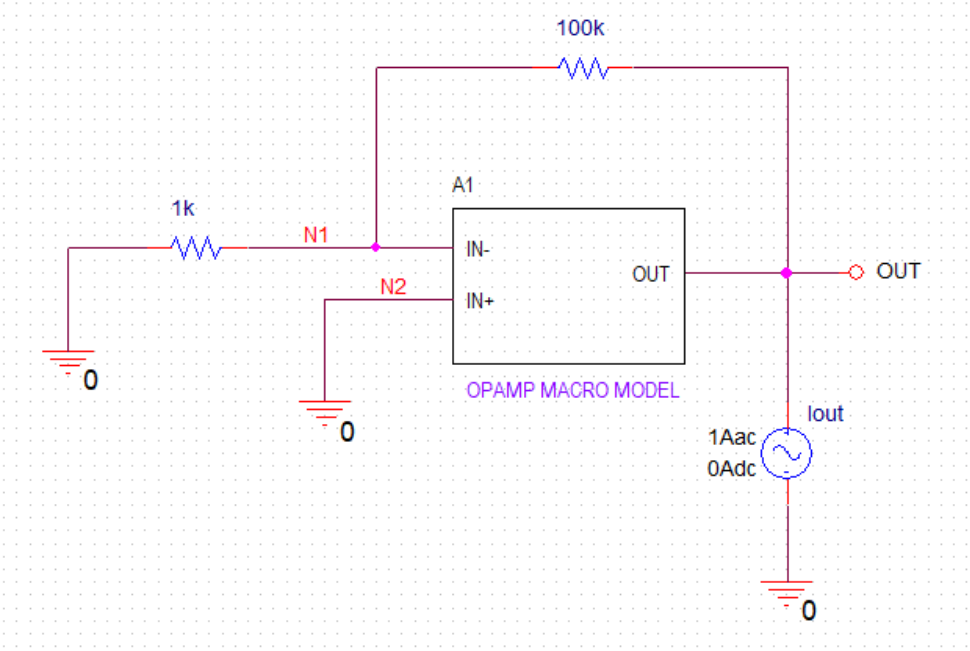


Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 2.1(b) (i), (ii), (iii)***************
******* Main circuit begins here**************
R1          N1 0   1k
Vin          N2 0 DC 0Vdc AC 1Vac
R2          N1 OUT   100k
X_A1          N2 N1 OUT OPAMP_MACRO
******* Main circuit ends here **************

******* Opamp macro model begins here **************
.SUBCKT OPAMP_MACRO     IN+ IN- OUT
Ro          OUT N3   75
VOS          N4 IN-  1m
Eb          N3 0 N2 0 1
Rb          N2 N1   16MEG
Cb          0 N2   1n
Ed          N1 0 IN+ N4 1E5
Rid          IN+ N4   2MEG
.ENDS
******* Opamp macro model ends here **************

******** Analysis begins here****************
.OP
.AC   DEC    20   0.1 10MEG
.PROBE
.END
******** Analysis ends here****************
```

The schematic sub-part (iv) is shown below

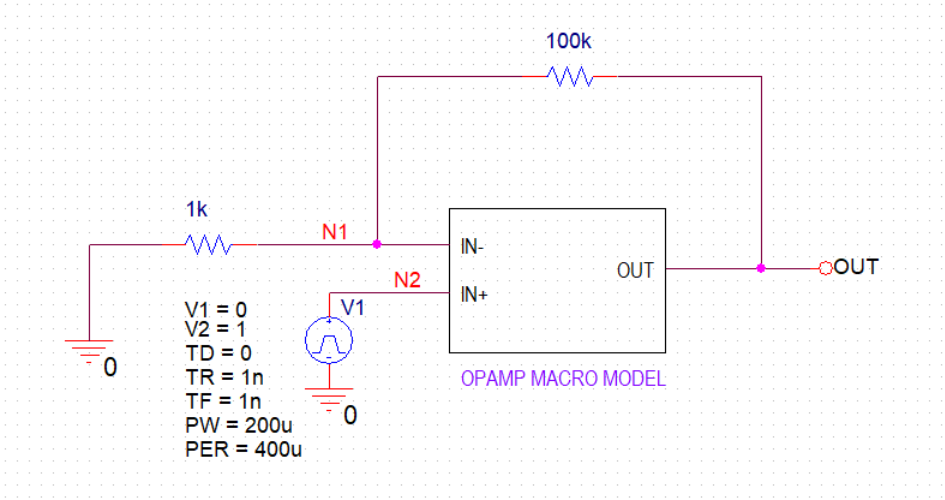


Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 2.1(b) (iv)***************
******* Main circuit begins here**************
Iout          OUT 0 DC 0Adc AC 1Aac
R2          N1 OUT  100k
R1          N1 0  1k
X_A1          0 N1 OUT OPAMP_MACRO
******* Main circuit ends here **************
******* Opamp macro model begins here **************
.SUBCKT OPAMP_MACRO    IN+ IN- OUT
Ro          OUT N3  75
VOS          N4 IN- 1m
Eb          N3 0 N2 0 1
Rb          N2 N1  16MEG
Cb          0 N2  1n
Ed          N1 0 IN+ N4 1E5
Rid          IN+ N4  2MEG
.ENDS
******* Opamp macro model ends here **************
******** Analysis begins here****************
.OP
.AC  DEC   20  0.1 10
.PROBE
.END
******** Analysis ends here****************
```

(c) The schematic for this part of the example is shown below.



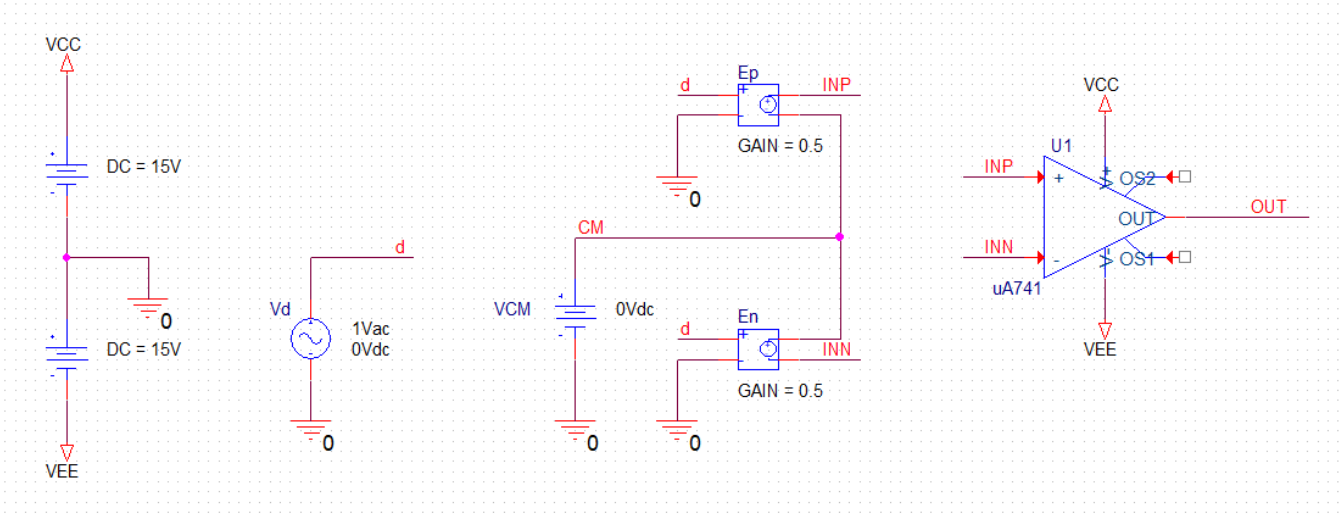
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 2.1(c) ***************
******* Main circuit begins here**************
V1          N2 0
+PULSE 0 1 10u 1n 1n 200u 400u
R1          N1 0  1k
R2          N1 OUT  100k
X_A1          N2 N1 OUT OPAMP_MACRO

******* Main circuit ends here **************
******* Opamp macro model begins here **************
.SUBCKT OPAMP_MACRO    IN+ IN- OUT
Ro          OUT N3  75
VOS          N4 IN- 1m
Eb          N3 0 N2 0 1
Rb          N2 N1  16MEG
Cb          0 N2  1n
Ed          N1 0 IN+ N4 1E5
Rid          IN+ N4  2MEG
.ENDS
******* Opamp macro model ends here **************
******** Analysis begins here****************
.TRAN 0.1uS 100uS
.PROBE
.END
******** Analysis ends here***************
```

Example S.2.2

The schematic of this example for calculation of AC gain is shown below



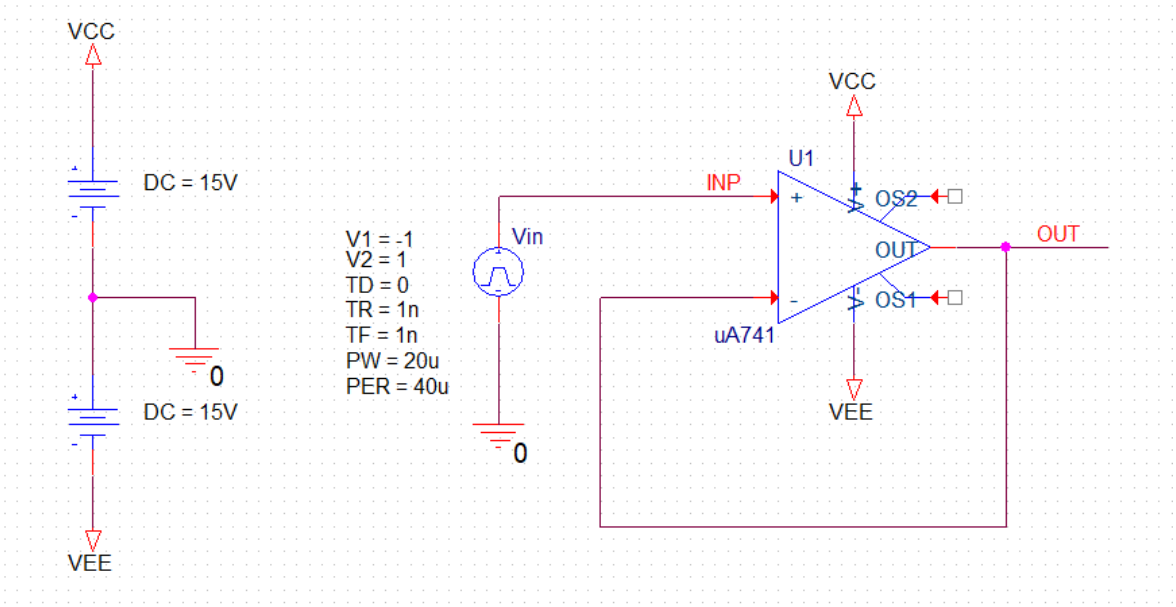
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 2.2 (AC Gain) ***************
******* Main circuit begins here**************
X_U1          INP INN VCC VEE OUT uA741
Ep          INP CM D 0 0.5
VCM          CM 0 0Vdc
Vd          D 0 DC 0Vdc AC 1Vac
VEE          0 VEE 15V
VCC          VCC 0 15V
En          CM INN D 0 0.5
******* Main circuit ends here **************
******** Model of uA741 begins here****************
* connections:   non-inverting input
*                |  inverting input
*                |  |  positive power supply
*                |  |  |  negative power supply
*                |  |  |  |  output
*                |  |  |  |  |
.subckt uA741    1 2 3 4 5
*
c1   11 12 8.661E-12
c2    6  7 30.00E-12
dc    5 53 dx
de   54  5 dx
dlp  90 91 dx
dln  92 90 dx
dp    4  3 dx
egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
fb    7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -10E6 10E6 10E6 -10E6
ga    6  0 11 12 188.5E-6
gcm   0  6 10 99 5.961E-9
```

```
iee   10   4 dc 15.16E-6
hlim 90   0 vlim 1K
q1    11   2 13 qx
q2    12   1 14 qx
r2     6   9 100.0E3
rc1    3 11 5.305E3
rc2    3 12 5.305E3
re1   13 10 1.836E3
re2   14 10 1.836E3
ree   10 99 13.19E6
ro1    8   5 50
ro2    7 99 100
rp     3   4 18.16E3
vb     9   0 dc 0
vc     3 53 dc 1
ve    54   4 dc 1
vlim   7   8 dc 0
vlp   91   0 dc 40
vln    0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=93.75)
.ends
******** Model of uA741 ends here***************
******** Analysis begins here***************
.AC  DEC   20   1 10MEG
.PROBE
.END
******** Analysis ends here***************
```

The schematic of this example for investigating SR limitations is shown below



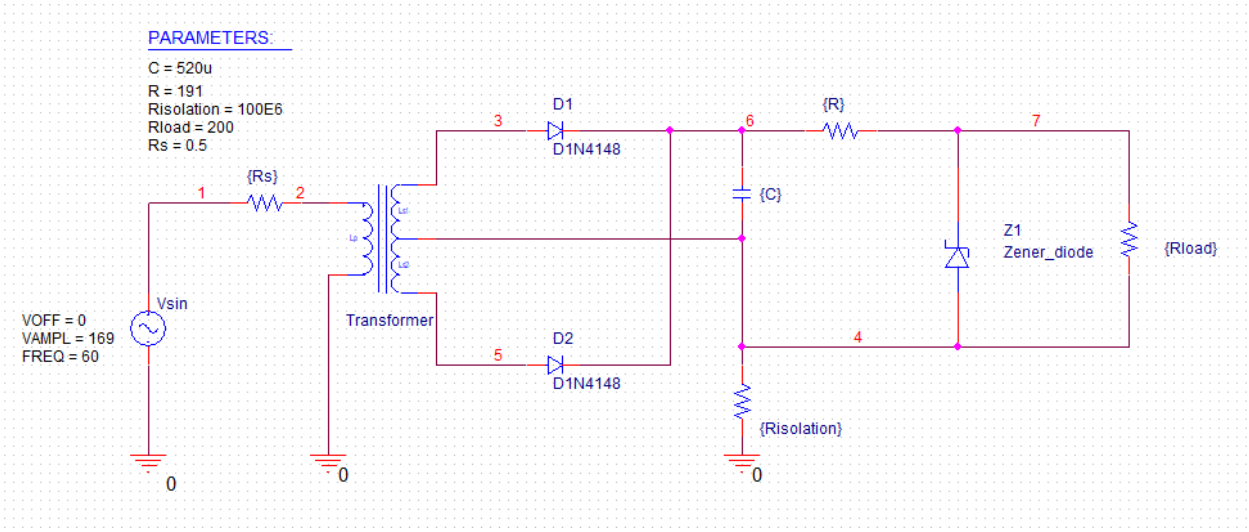
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 2.2 (Slew Rate) ***************
******* Main circuit begins here**************

X_U1          INP OUT VCC VEE OUT uA741
Vin          INP 0
+PULSE -1 1 0 1n 1n 20u 40u
VEE          0 VEE 15V
VCC          VCC 0 15V
******* Main circuit ends here **************
******** Model of uA741 begins here****************
* connections:   non-inverting input
*                |  inverting input
*                |  |  positive power supply
*                |  |  |  negative power supply
*                |  |  |  |  output
*                |  |  |  |  |
.subckt uA741    1 2 3 4 5
*
c1   11 12 8.661E-12
c2    6  7 30.00E-12
dc    5 53 dx
de   54  5 dx
dlp  90 91 dx
dln  92 90 dx
dp    4  3 dx
egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
fb    7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -10E6 10E6 10E6 -10E6
ga    6  0 11 12 188.5E-6
gcm   0  6 10 99 5.961E-9
iee  10  4 dc 15.16E-6
hlim 90  0 vlim 1K
q1   11  2 13 qx
q2   12  1 14 qx
r2    6  9 100.0E3
rc1   3 11 5.305E3
rc2   3 12 5.305E3
re1  13 10 1.836E3
re2  14 10 1.836E3
ree  10 99 13.19E6
ro1   8  5 50
ro2   7 99 100
rp    3  4 18.16E3
vb    9  0 dc 0
vc    3 53 dc 1
ve   54  4 dc 1
vlim  7  8 dc 0
vlp  91  0 dc 40
vln   0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=93.75)
.ends
******** Model of uA741 ends here****************
******** Analysis begins here****************
.TRAN  0.01uS  80uS
.PROBE
.END
******** Analysis ends here***************
```

Example S.4.1

The schematic of this example is shown below.



Netlist:

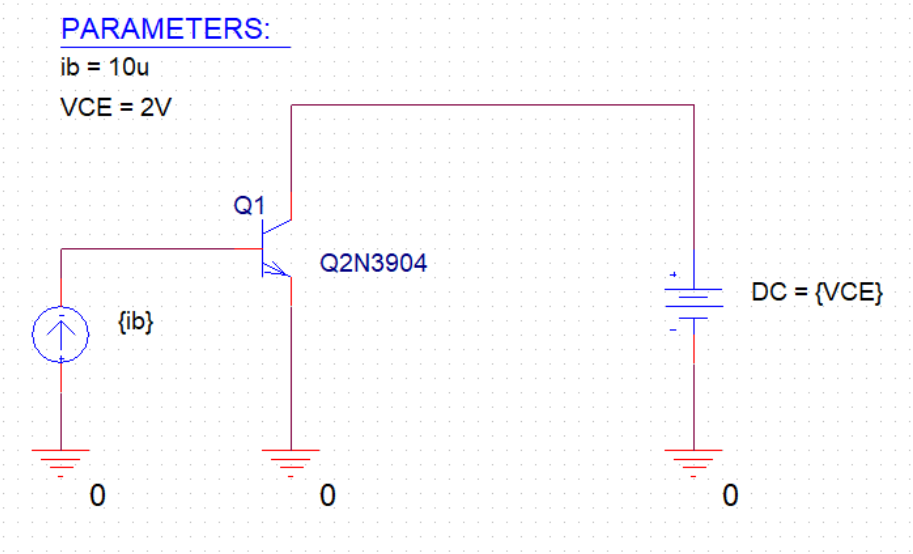
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 4.1 ***************
******* Main circuit begins here**************
D1          3 6 D1N4148
D2          5 6 D1N4148
R3          7 4  {Rload}
Vsin          1 0
+SIN 0 169 60 0 0 0
C1          4 6  {C}
R1          7 6  {R}
X_Z1          4 7 ZENER_DIODE
R4          4 0  {Risolation}
R2          2 1  {Rs}
X_TX1          0 2 3 4 5 TX
.PARAM  rs=0.5 risolation=100e6 c=520u rload=200 r=191
******* Main circuit ends here **************


******** Model of ZENER DIODE begins here****************
.SUBCKT ZENER_DIODE 1 2
*connections:       | |
*              andode |
*               cathode
Dforward 1 2 1mA_diode
Dreverse 2 4 ideal_diode
Vz0 4 3 DC 4.9V
Rz 1 3 10
* diode model statements
.model 1mA_diode D (Is=100pA n=1.679)
.model ideal_diode D (Is=100pA n=0.01)
.ends ZENER_DIODE
******** Model of ZENER DIODE ends here****************
```

```
******** Model of 1N4148 Diode (from EVAL library in PSpice) begins here****************
.model D1N4148  D(Is=2.682n N=1.836 Rs=.5664 Ikf=44.17m Xti=3 Eg=1.11 Cjo=4p
+               M=.3333 Vj=.5 Fc=.5 Isr=1.565n Nr=2 Bv=100 Ibv=100u Tt=11.54n)
******** Model of 1N4148 Diode (from EVAL library in PSpice) ends here****************

******** Model of Nonlinear Transformer with Center-Tapped Secondary begins here****************
.subckt TX 1 2 3 4 5 Params:
Lp 2 1 10mH
Ls1 3 4 52uH
Ls2 4 5 52uH
K1 Lp Ls1 0.999
K2 Lp Ls2 0.999
K3 Ls1 Ls2 0.999
.ends TX
******** Model of Nonlinear Transformer with Center-Tapped Secondary ends here****************

******** Analysis begins here****************
.TRAN   0.1mS  200mS
.PROBE
.END
******** Analysis ends here****************
```

Example S.6.1

The schematic of this example is shown below.



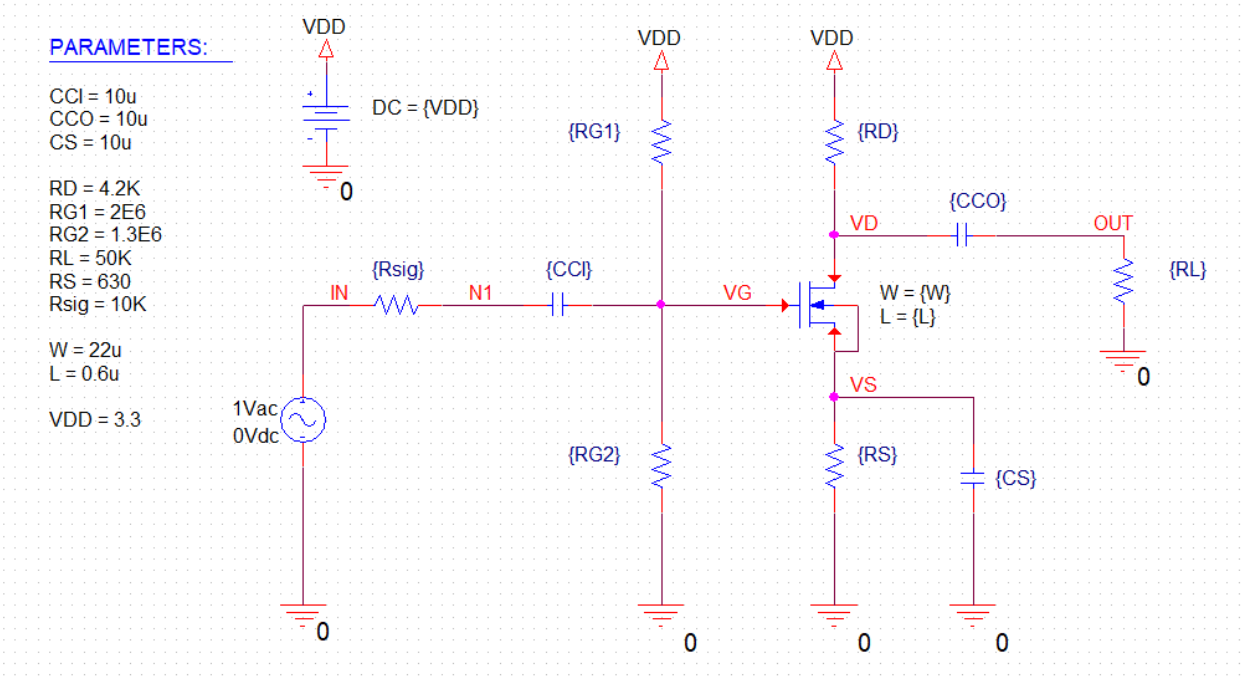
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 6.1 ***************
******* Main circuit begins here**************
Q1          N111317 N111357 0 Q2N3904
V1          N111317 0 {VCE}
Ibase          0 N111357 DC {ib}
.PARAM  ib=10u vce=2v
******* Main circuit ends here**************
**************Model for 2N3904 NPN BJT (from Eval library in Pspice) begins here***********
.model Q2N3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+               Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+               Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
**************Model for 2N3904 NPN BJT (from Eval library in Pspice) ends here***********
******** Analysis begins here****************
.DC [LIN] Ibase  1u 200u 1u
.PROBE
.END
******** Analysis ends here***************
```

Example S.7.1

The schematic of this example is shown below.



Netlist:

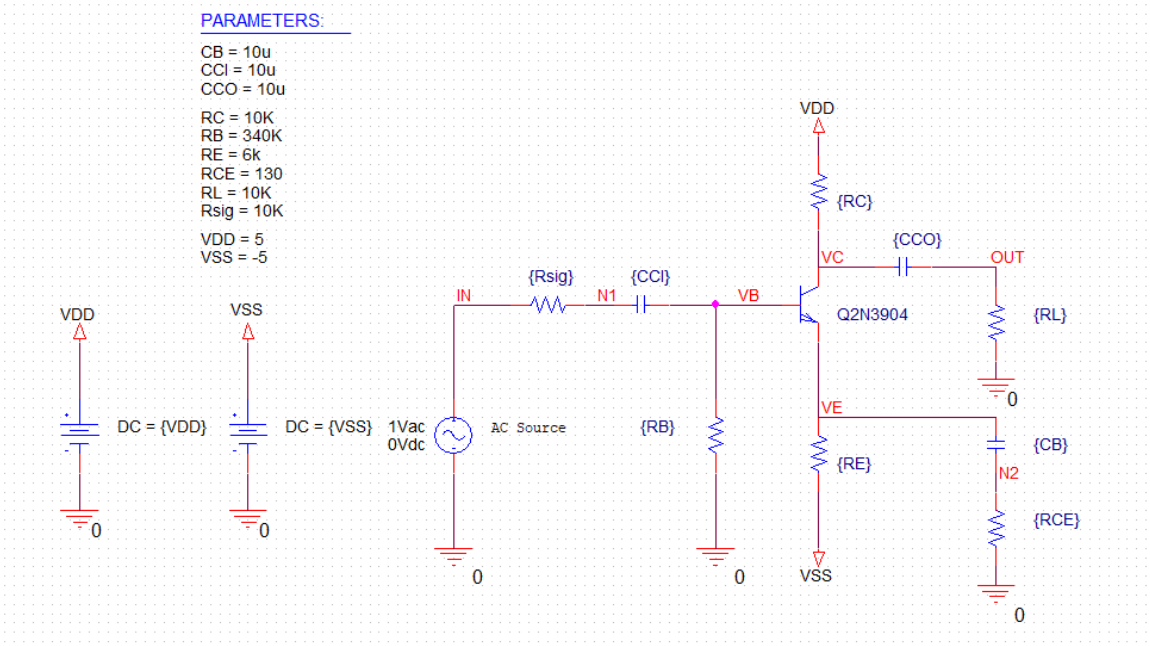
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 7.1 ***************
******* Main circuit begins here**************
M2          VD VG VS VS NMOS0P5
+ L={L}
+ W={W}
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=1
R11          VG VDD  {RG1}
R16          0 VS  {RS}
R15          0 VG  {RG2}
R12          VD VDD  {RD}
C6          0 VS  {CS}
C4          VD OUT  {CCO}
R14          IN N1  {Rsig}
C5          N1 VG  {CCI}
R13          0 OUT  {RL}
V3          IN 0 DC 0Vdc AC 1Vac
V1          VDD 0 {VDD}
.PARAM  RS=630 CS=10u L=0.6u CCO=10u VDD=3.3 CCI=10u RG1=2e6 RL=50k RG2=1.3e6
+  RSIG=10k W=22u RD=4.2k
******* Main circuit ends here**************
```

```
************Model for NMOS in 0.5um CMOS Technology begins here*****************************
*               (created by Anas Hamoui & Olivier Trescases)
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+               LD=0.08E-06 WD=0 UO=460 LAMBDA=0.1 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
************Model for NMOS in 0.5um CMOS Technology ends here*****************************

******** Analysis begins here****************
.OP
.AC  DEC   20  10m 10G
.PROBE
.END
******** Analysis ends here***************
```

Example S.7.2

The schematic of this example is shown below.



Netlist:

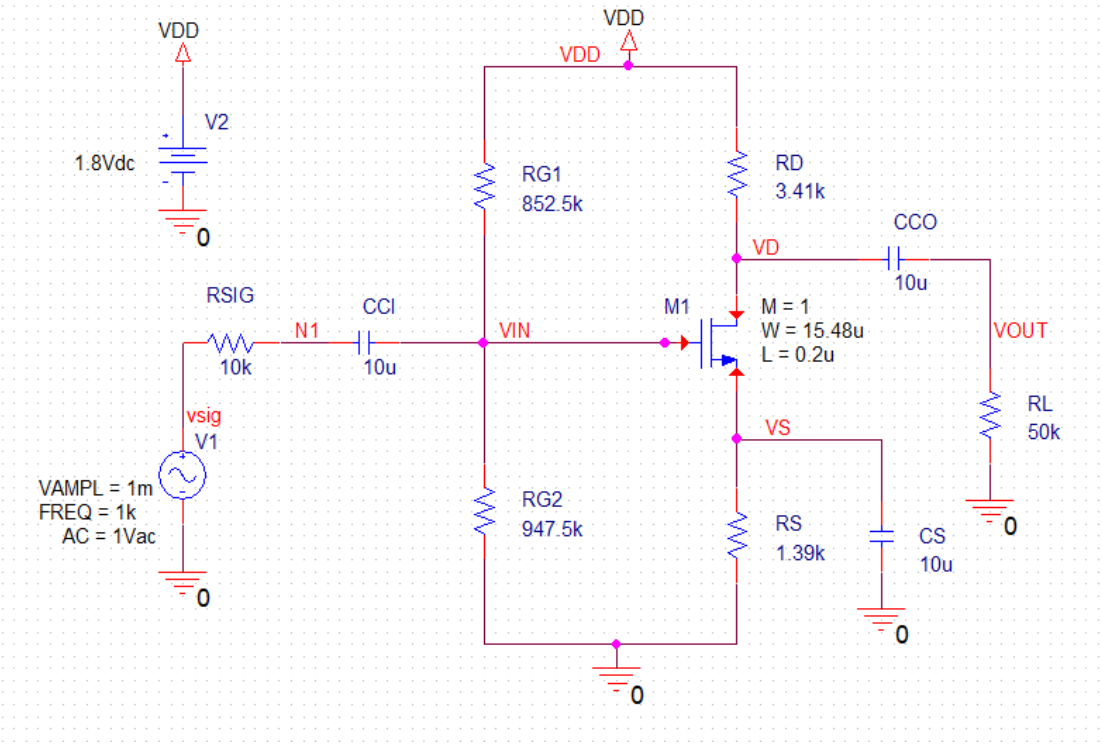
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 7.2 ***************
******* Main circuit begins here**************
C2          N1 VB   {CCI}
R7          0 VB   {RB}
V5          IN 0 DC 0Vdc AC 1Vac
Q2          VC VB VE Q2N3904
V7          VSS 0 {VSS}
R4          VC VDD   {RC}
R9          0 N2   {RCE}
R8          VSS VE   {RE}
C1          VC OUT   {CCO}
C3          N2 VE   {CB}
R6          0 OUT   {RL}
R5          IN N1   {Rsig}
V6          VDD 0 {VDD}
.PARAM   rc=10k cb=10u re2=1 vss=-5 rb=340k re1=6k cco=10u vdd=5 cci=10u rl=10k
+   rsig=10k rx=1 re=6k rce=130
******* Main circuit ends here**************

**************Model for 2N3904 NPN BJT (from Eval library in Pspice) begins here***********
.model Q2N3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+               Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+               Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
**************Model for 2N3904 NPN BJT (from Eval library in Pspice) ends here***********
```

```
******** Analysis begins here****************
.OP
.AC  DEC   20  1 10MEG
.PROBE
.END
******** Analysis ends here****************
```

Example S.7.3

The schematic of this example for finding Av is shown below.



Netlist:

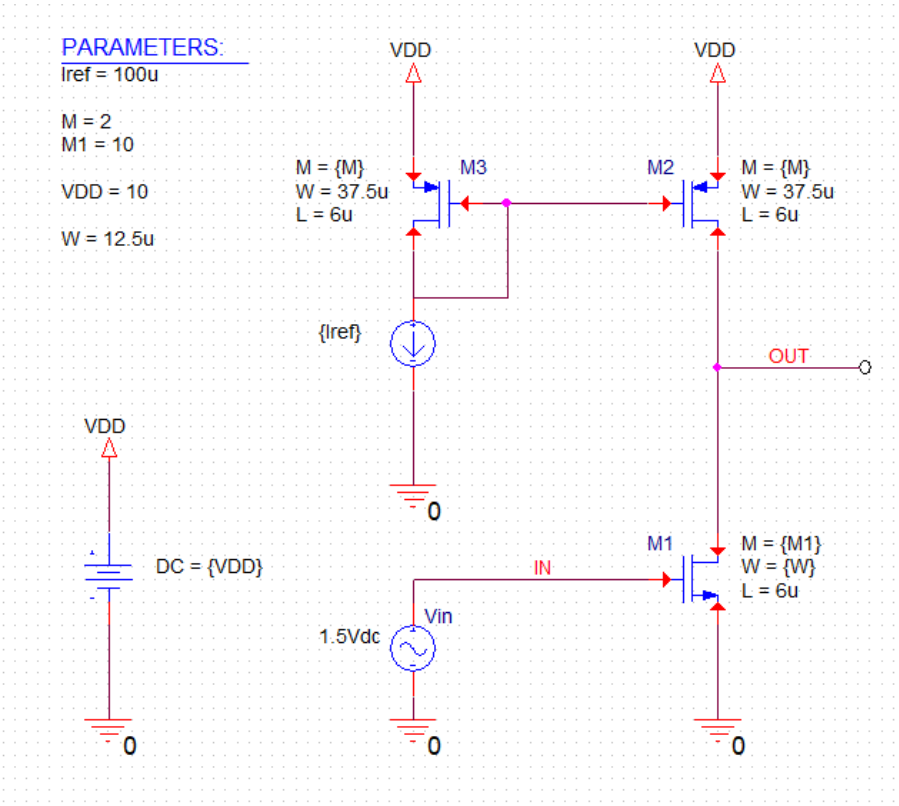
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 7.3  ***********************
******* Main circuit begins here**************
R_RG1          VIN VDD  852.5k TC=0,0
R_RG2          0 VIN  947.5k TC=0,0
M_M1          VD VIN VS 0 NMOS4
+ L=0.2u
+ W=15.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=1
R_RD          VD VDD  3.41k TC=0,0
R_RS          0 VS  1.39k TC=0,0
R_RL          0 VOUT  50k TC=0,0
C_CCO          VD VOUT  10u  TC=0,0
C_CS          0 VS  10u  TC=0,0
C_CCI          N1 VIN  10u  TC=0,0
V_V1          VSIG 0  AC 1Vac
+SIN 0 1m 1k 0 0 0
R_RSIG          N1 VSIG  10k TC=0,0
V_V2          VDD 0 1.8Vdc
```

```
******* Main circuit ends here**************

*****************NMOS models begin here*********************
.model NMOS4   NMOS(LEVEL= 1 VTO=0.45 GAMMA= 0.3  PHI=0.84
+ LAMBDA= 0.08
+ RS=    0.0
+ RD=    0.0
+ CBD=   0.0
+ CBS=   0.0
+ IS=    1.0e-14
+ PB=    0.9
+ CGSO=  0.3665e-9
+ CGDO=   0.3665e-9
+ CGBO=   0.38e-9
+ RSH=   0
+ CJ=    1.6e-3
+ MJ=    0.5
+ CJSW=  2.0405e-10
+ MJSW=  0.200379
+ JS=    8.38e-6
+ TOX= 4.08e-09
+ NSS=   0.0
+ TPG=   1.0
+ LD=    10e-9
+ U0 = 291
+ KF=    0.0
+ AF=    1.0
+ FC=    0.5
+ TNOM=  27
+ )
*****************NMOS models end here*********************

******** Analysis begins here****************
.OP
.TRAN 0.01m 2.5m
.PROBE
.END
******** Analysis ends here****************
```

Example S.8.1

The schematic of this example is shown below.



Netlist:

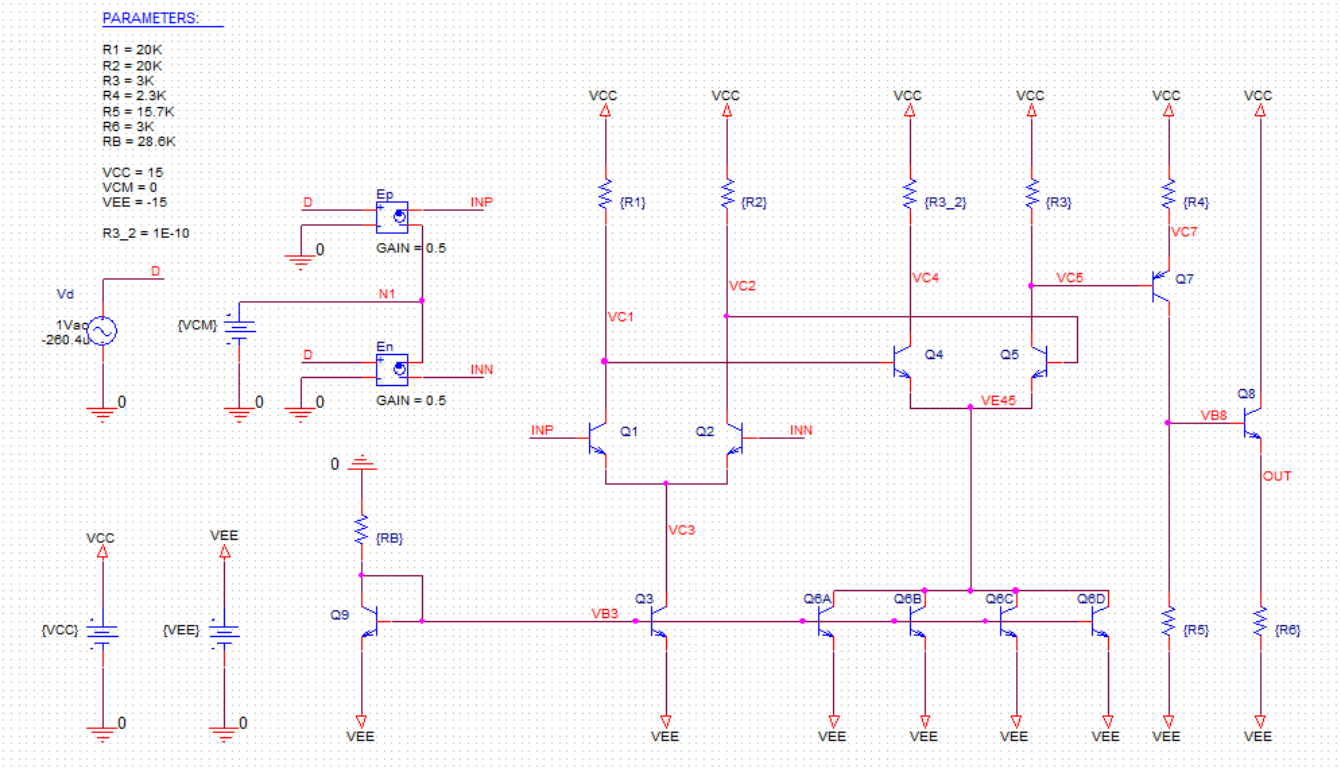
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 8.1 ***************
******* Main circuit begins here**************
M1          OUT IN 0 0 NMOS5P0
+ L=6u
+ W={W}
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M1}
V2          VDD 0 {VDD}
M3          VG23 VG23 VDD VDD PMOS5P0
+ L=6u
+ W=37.5u
+ AD=1.72E-10
+ AS=1.72E-10
+ PD=5.25e-5
+ PS=5.25E-5
+ M={M}
I2          VG23 0 DC {Iref}
```

```
V_Vin         IN 0 DC 1.5Vdc AC 1Vac
M2          OUT VG23 VDD VDD PMOS5P0
+ L=6u
+ W=37.5u
+ AD=1.72E-10
+ AS=1.72E-10
+ PD=5.25e-5
+ PS=5.25E-5
+ M={M}
.PARAM  iref=100u m=2 vdd=10 m1=10 w=12.5u
******* Main circuit ends here**************
***************Model for NMOS in 5um CMOS Technology begins here*********************
*               (created by Anas Hamoui & Olivier Trescases)
.model NMOS5P0 NMOS(Level=1 VTO=1 GAMMA=1.4 PHI=0.7
+               LD=0.7E-06 WD=0 UO=750 LAMBDA=0.01 TOX=85E-9 PB=0.7 CJ=0.4E-3
+               CJSW=0.8E-9 MJ=0.5 MJSW=0.5 CGDO=0.4E-9 JS=1E-6 CGBO=0.2E-9
+               CGSO=0.4E-9)
***************Model for NMOS in 5um CMOS Technology ends here*********************
***************Model for PMOS in 5um CMOS Technology begins here*********************
*               (created by Anas Hamoui & Olivier Trescases)
.model PMOS5P0 PMOS(Level=1 VTO=-1 GAMMA=0.65 PHI=0.65
+               LD=0.6E-06 WD=0 UO=250 LAMBDA=0.03 TOX=85E-9 PB=0.7 CJ=0.18E-3
+               CJSW=0.6E-9 MJ=0.5 MJSW=0.5 CGDO=0.4E-9 JS=1E-6 CGBO=0.2E-9
+               CGSO=0.4E-9)
***************Model for PMOS in 5um CMOS Technology ends here*********************

******** Analysis begins here****************
.DC [LIN] V_Vin  0 10 0.05
.PROBE
.END
******** Analysis ends here****************
```

Example S.9.1

The schematic of this example is shown below.



Netlist:

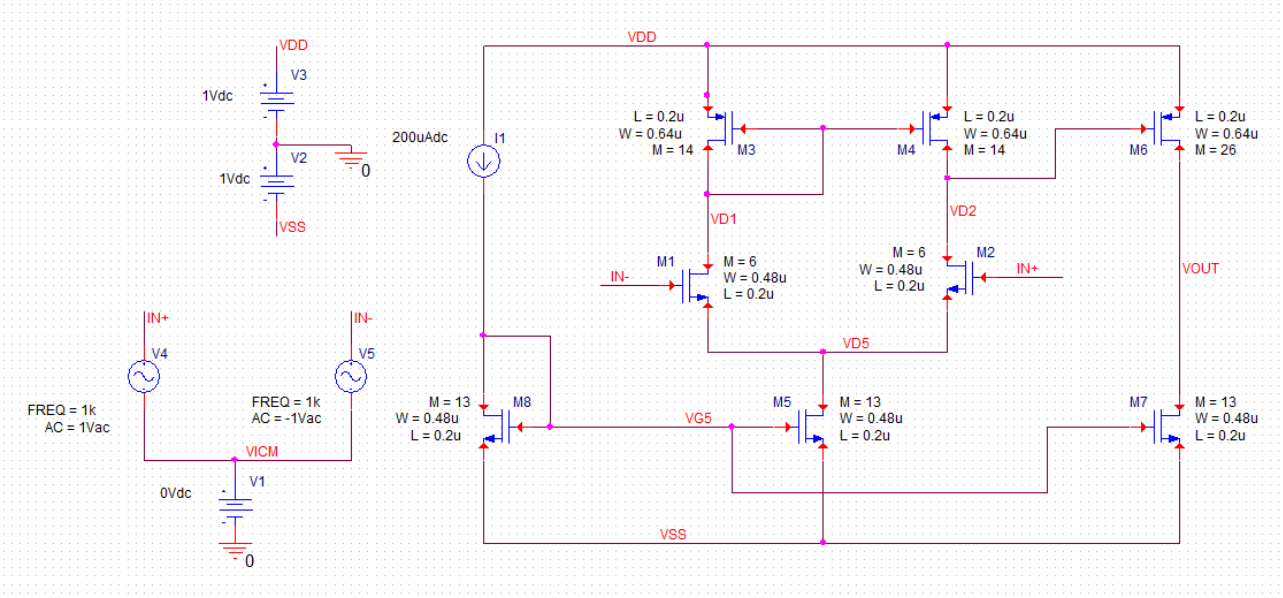
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 9.1 ***************
******* Main circuit begins here**************
Q_Q2          VC2 INN VC3 Q2N3904
Q_Q1          VC1 INP VC3 Q2N3904
R_R3          VC5 VCC  {R3}
R_R5          VEE VB8  {R5}
Q_Q5          VC5 VC2 VE45 Q2N3904
Q_Q4          VC4 VC1 VE45 Q2N3904
R_R4          VC7 VCC  {R4}
R_RB          VB3 0  {RB}
Q_Q6A          VE45 VB3 VEE Q2N3904
Q_Q6D          VE45 VB3 VEE Q2N3904
V_VCC          VCC 0 {VCC}
V_Vd          D 0 DC -260.4u AC 1Vac
Q_Q6B          VE45 VB3 VEE Q2N3904
V_VEE          VEE 0 {VEE}
E_En          N1 INN D 0 0.5
Q_Q8          VCC VB8 OUT Q2N3904
Q_Q9          VB3 VB3 VEE Q2N3904
R_R2          VC2 VCC  {R2}
R_R1          VC1 VCC  {R1}
```

```
Q_Q3          VC3 VB3 VEE Q2N3904
Q_Q7          VB8 VC5 VC7 Q2N3906
R_R6          VEE OUT  {R6}
R_R7          VC4 VCC  {R3_2}
Q_Q6C          VE45 VB3 VEE Q2N3904
E_Ep          INP N1 D 0 0.5
V_VCM          N1 0 {VCM}
.PARAM  vcm=0 rb=28.6k vee=-15 r6=3k r5=15.7k r3_2=1e-10 r4=2.3k r3=3k r2=20k
+  vcc=15 r1=20k
******* Main circuit ends here**************

**************Model for 2N3904 NPN BJT (from Eval library in Pspice) begins here***********
.model Q2N3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+               Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+               Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
**************Model for 2N3904 NPN BJT (from Eval library in Pspice) ends here***********

**************Model for 2N3906 NPN BJT (from Eval library in Pspice) begins here***********
.model Q2N3906 PNP(Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=180.7 Ne=1.5 Ise=0
+               Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p
+               Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n
+               Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)
**************Model for 2N3906 NPN BJT (from Eval library in Pspice) begins here***********
******** Analysis begins here****************
.OP
.DC [LIN] V_Vd  -15 15 0.1
*.AC  DEC   20  1 1G
*.DC [LIN] V_VCM  -15 15 0.1
.PROBE
.END
******** Analysis ends here****************
```

Example S.9.2

The schematic of this example is shown below.



Netlist:

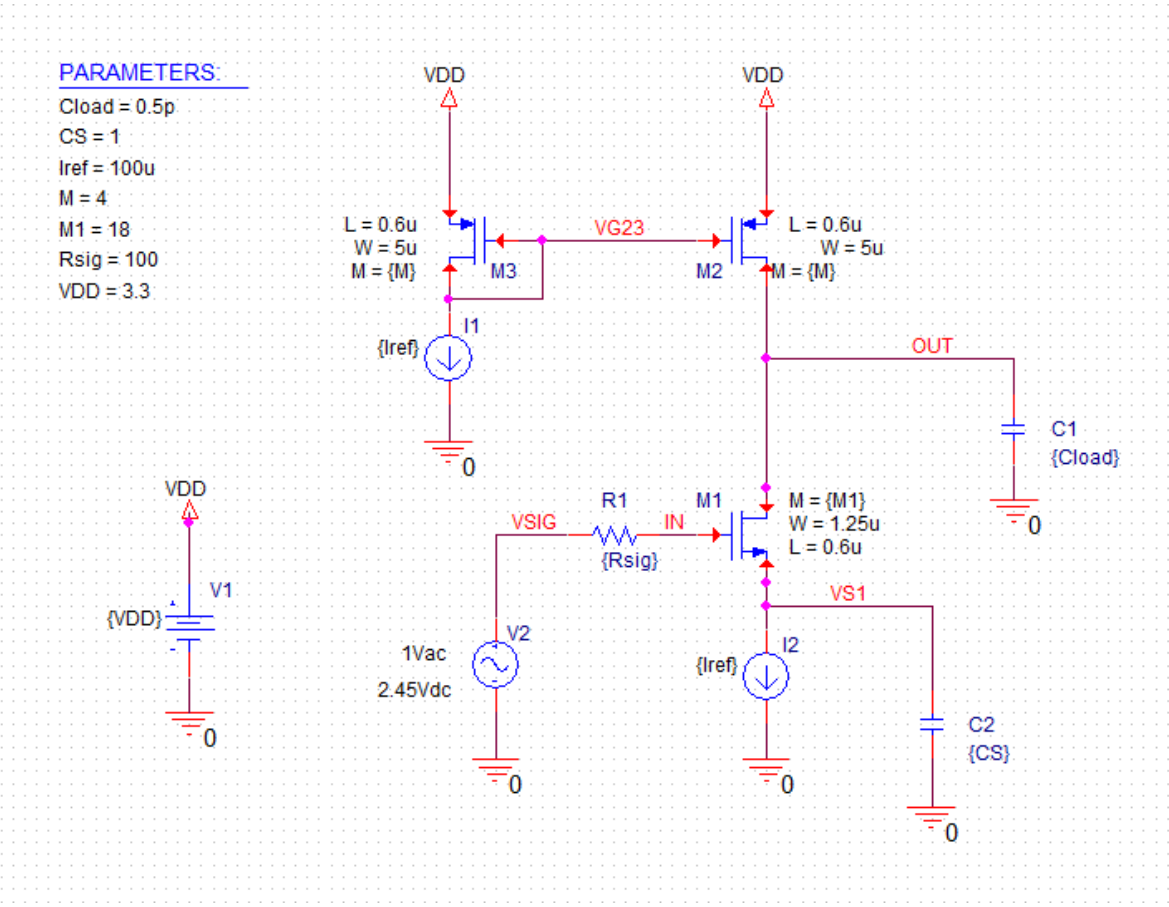
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 9.2 ***********************
******* Main circuit begins here**************
M_M4          VD2 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=14
M_M3          VD1 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=14
M_M1          VD1 IN- VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=6
M_M2          VD2 IN+ VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
```

```
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=6
M_M5          VD5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=13
M_M7          VOUT VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=13
M_M6          VOUT VD2 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=26
M_M8          VG5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=13
I_I1          VDD VG5 DC 200uAdc
V_V2          0 VSS 1Vdc
V_V1          VICM 0 0Vdc
V_V3          VDD 0 1Vdc
V_V4          IN+ VICM  AC 1Vac
+SIN 0 1m 1k 0 0 0
V_V5          IN- VICM  AC -1Vac
+SIN 0 1m 1k 0 0 0
******* Main circuit ends here**************
*****************PMOS and NMOS models begin here*********************
.model PMOS4   PMOS(Level=1 VTO=-0.5 GAMMA=0.3 PHI=0.8
+               LD=0.01E-06 WD=0 UO=132 LAMBDA=0.11 TOX=5E-9 PB=0.9 CJ=0.93E-3
+               CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+               CGSO=0.35E-9)
.model NMOS4   NMOS(Level=1 VTO=0.5 GAMMA=0.3 PHI=0.8
+               LD=0.01E-06 WD=0 UO=370 LAMBDA=0.08 TOX=5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
*****************PMOS and NMOS models end here*********************
******** Analysis begins here****************
.DC [LIN] V_V1  -1.0 1.0 100m
*.AC  DEC   20  1 10K
*.DC LIN V_V5 -750u 400u 20u

.PROBE
.END
******** Analysis ends here****************
```

Example S.10.1

The schematic of the CS amplifier of this example is shown below.



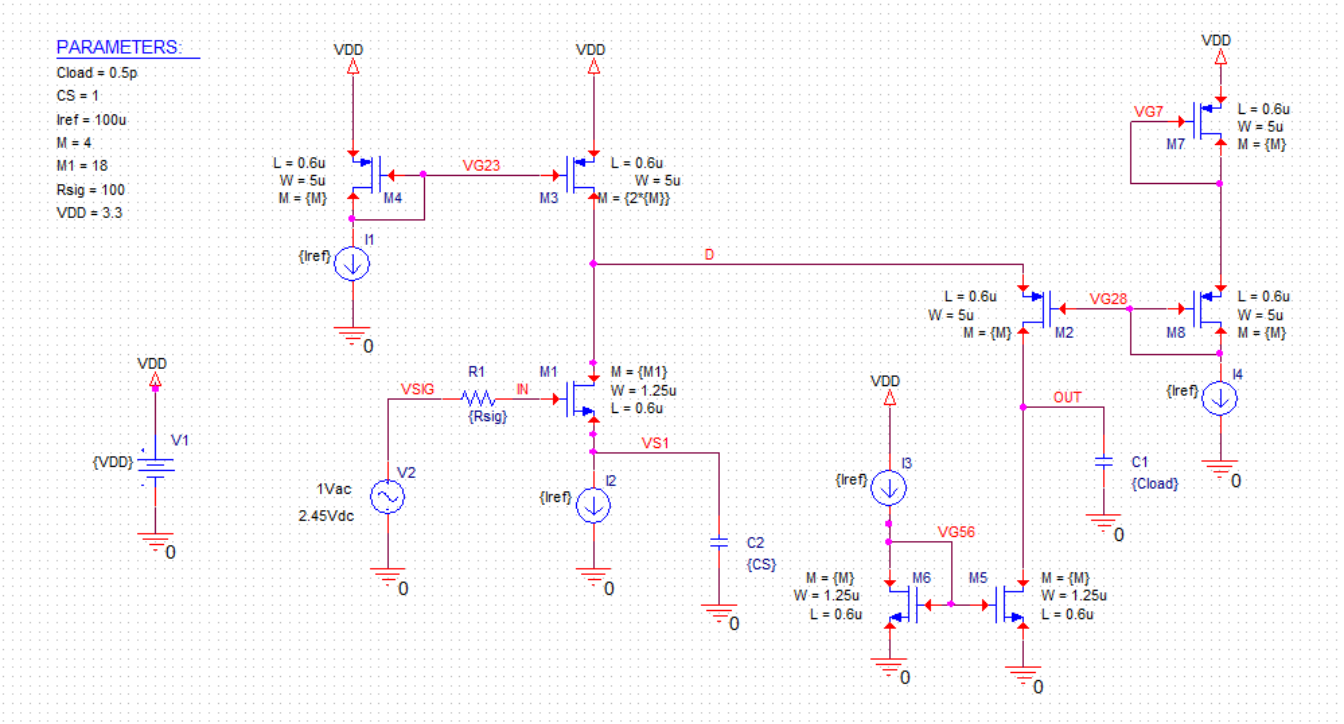
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 10.1 CS amplifier *********
******* Main circuit begins here**************
M_M1          OUT IN VS1 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M1}
I_I1          VG23 0 DC {Iref}
I_I2          VS1 0 DC {Iref}
V_V1          VDD 0 {VDD}
R_R1          VSIG IN  {Rsig} TC=0,0
C_C1          0 OUT  {Cload}  TC=0,0
C_C2          0 VS1  {CS}  TC=0,0
```

```
M_M3          VG23 VG23 VDD VDD PMOS0P5
+ L=0.6u
+ W=5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M}
M_M2          OUT VG23 VDD VDD PMOS0P5
+ L=0.6u
+ W=5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M}
V_V2          VSIG 0  AC 1Vac
+SIN 2.45Vdc 1 1k 0 0 0
.PARAM  iref=100u cs=1 m=4 vdd=3.3 cload=0.5p rsig=100 m1=18
******* Main circuit ends here**************

************Model for NMOS in 0.5um CMOS Technology begins here*****************
*              (created by Anas Hamoui & Olivier Trescases)
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+               LD=0.08E-06 WD=0 UO=460 LAMBDA=0.1 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
************Model for NMOS in 0.5um CMOS Technology ends here*****************

************Model for PMOS in 0.5um CMOS Technology begins here*****************
*              (created by Anas Hamoui & Olivier Trescases)
.model PMOS0P5 PMOS(Level=1 VTO=-0.8 GAMMA=0.45 PHI=0.8
+               LD=0.09E-06 WD=0 UO=115 LAMBDA=0.2 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+               CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+               CGSO=0.35E-9)
************Model for PMOS in 0.5um CMOS Technology ends here*****************

******** Analysis begins here****************
.OP
.AC  DEC   20  1 1G
.PROBE
.END
******** Analysis ends here****************
```

The schematic of the folded-cascode amplifier of this example is shown below



Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

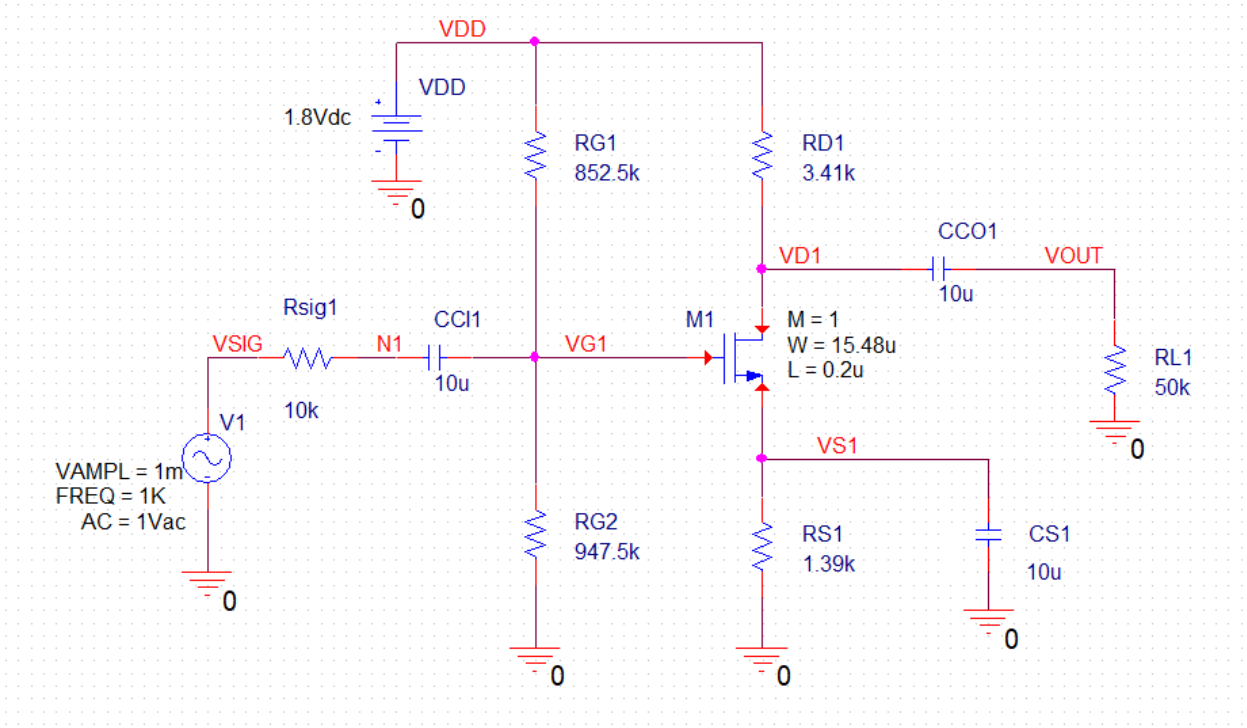
```
********Example S 10.1 folded-cascode amplifier *********
******* Main circuit begins here**************
I_I2          VS1 0 DC {Iref}
I_I1          VG23 0 DC {Iref}
M_M3          D VG23 VDD VDD PMOS0P5
+ L=0.6u
+ W=5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={2*{M}}
R_R1          VSIG IN  {Rsig} TC=0,0
C_C2          0 VS1  {CS}  TC=0,0
V_V2          VSIG 0  AC 1Vac
+SIN 2.45Vdc 1 1k 0 0 0
M_M1          D IN VS1 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
```

```
+ M={M1}
M_M4          VG23 VG23 VDD VDD PMOS0P5
+ L=0.6u
+ W=5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M}
V_V1          VDD 0 {VDD}
C_C1          0 OUT  {Cload}  TC=0,0
M_M2          OUT VG28 D VDD PMOS0P5
+ L=0.6u
+ W=5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M}
M_M7          VG7 VG7 VDD VDD PMOS0P5
+ L=0.6u
+ W=5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M}
M_M8          VG28 VG28 VG7 VDD PMOS0P5
+ L=0.6u
+ W=5u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M}
I_I3          VDD VG56 DC {Iref}
I_I4          VG28 0 DC {Iref}
M_M5          OUT VG56 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M}
M_M6          VG56 VG56 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M}
.PARAM  iref=100u cs=1 m=4 vdd=3.3 cload=0.5p rsig=100 m1=18
******* Main circuit ends here**************

************Model for NMOS in 0.5um CMOS Technology begins here*****************
*               (created by Anas Hamoui & Olivier Trescases)
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+               LD=0.08E-06 WD=0 UO=460 LAMBDA=0.1 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
************Model for NMOS in 0.5um CMOS Technology ends here*****************
```

```
************Model for PMOS in 0.5um CMOS Technology begins here*****************
*              (created by Anas Hamoui & Olivier Trescases)
.model PMOS0P5 PMOS(Level=1 VTO=-0.8 GAMMA=0.45 PHI=0.8
+              LD=0.09E-06 WD=0 UO=115 LAMBDA=0.2 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+              CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+              CGSO=0.35E-9)
************Model for PMOS in 0.5um CMOS Technology ends here*****************

******** Analysis begins here****************
.OP
.AC  DEC   20  1 1G
.PROBE
.END
******** Analysis ends here***************
```

Example S.10.2

The schematic of this example is shown below.



Netlist:

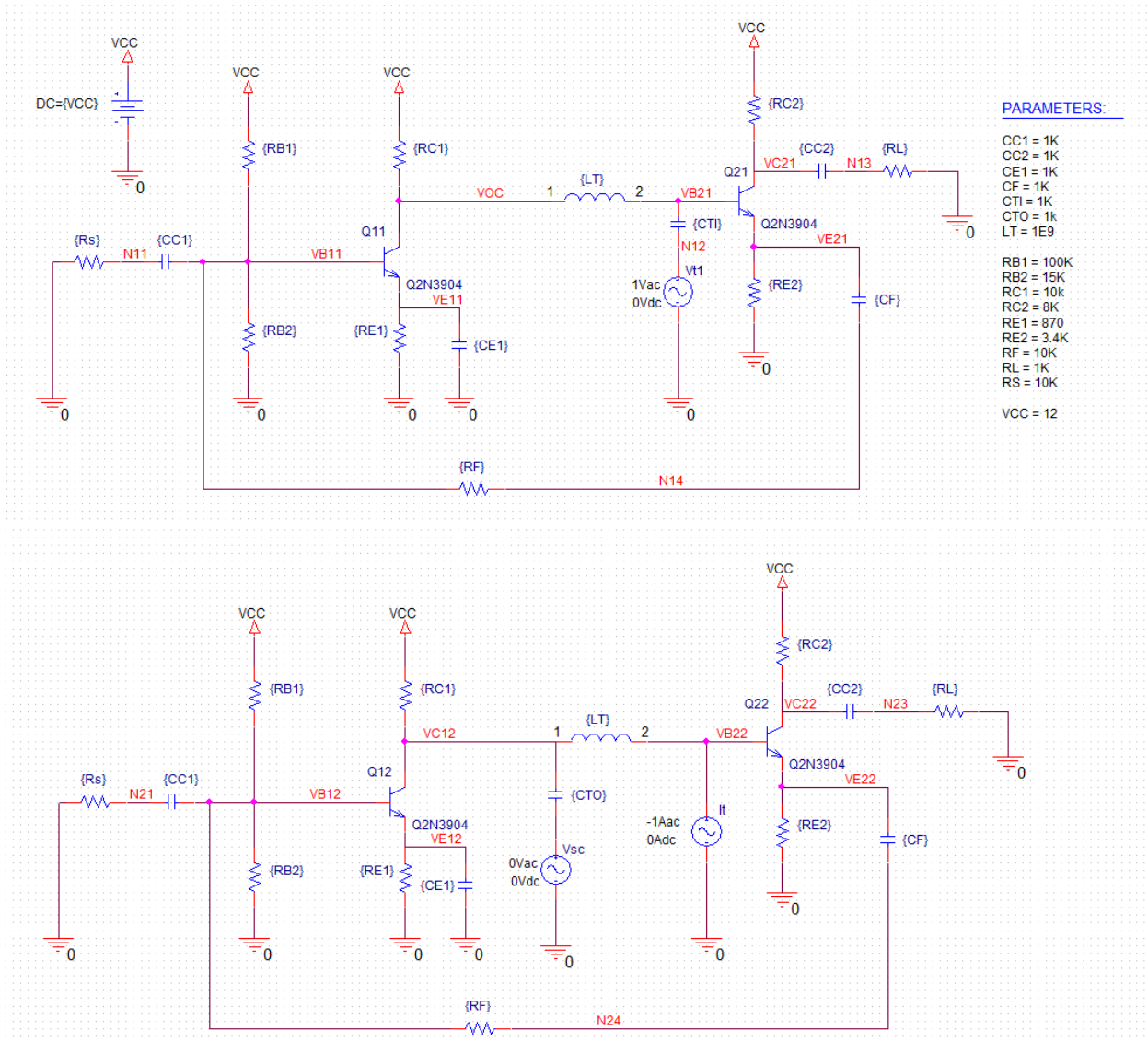
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 10.2 ***********************
******* Main circuit begins here**************
M_M1          VD1 VG1 VS1 0 NMOS4
+ L=0.2u
+ W=15.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=1
R_RG1          VG1 VDD  852.5k TC=0,0
R_RG2          0 VG1  947.5k TC=0,0
R_RD1          VD1 VDD  3.41k TC=0,0
R_RS1          0 VS1  1.39k TC=0,0
R_RL1          0 VOUT  50k TC=0,0
R_Rsig1          N1 VSIG  10k TC=0,0
C_CCI1          N1 VG1  10u  TC=0,0
C_CCO1          VD1 VOUT  10u  TC=0,0
V_V1          VSIG 0  AC 1Vac
+SIN 0 1m 1K 0 0 0
V_VDD          VDD 0 1.8Vdc
C_CS1          0 VS1  10u  TC=0,0
******* Main circuit ends here**************
```

```
*****************NMOS models end here*********************
.model NMOS4    NMOS(Level=1 VTO=0.45 GAMMA=0.3 PHI=0.8
+               LD=0.01E-06 WD=0 UO=370 LAMBDA=0.08 TOX=5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
*****************NMOS models end here*********************

******** Analysis begins here****************
.OP
.AC  DEC   20  10m 10G
.PROBE
.END
******** Analysis ends here****************
```

Example S.11.1

The schematic of this example using method 1 is shown below.



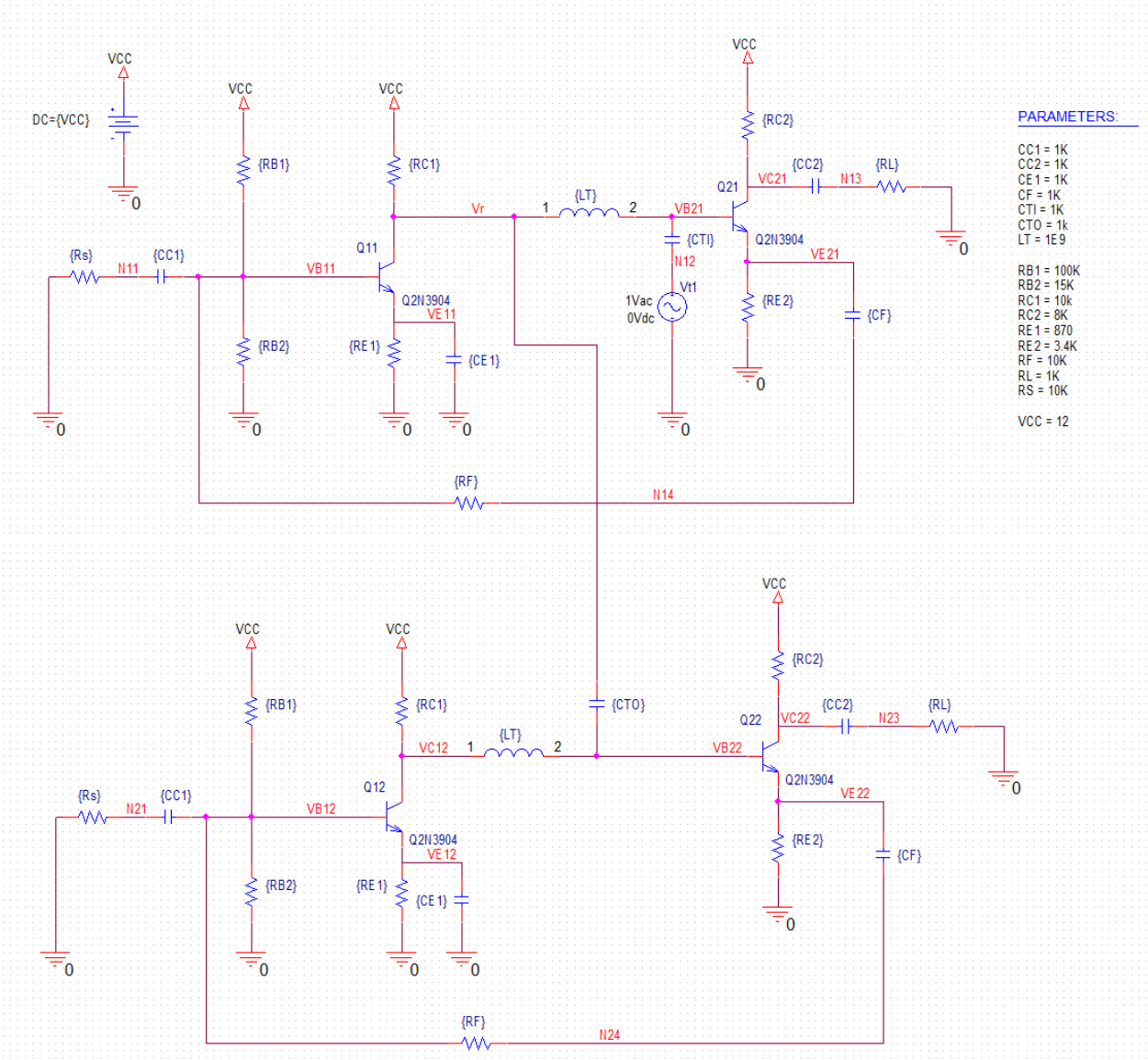
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
******Example S 11.1 Method 1 *************
******* Main circuit begins here**************
R_Rb8          0 VB12   {RB2}
R_RF3          N24 VB12   {RF}
R_Rb7          VB12 VCC   {RB1}
C_CC7          VC22 N23   {CC2}
```

```
Q_Q22          VC22 VB22 VE22 Q2N3904
L_LT3          VOC VB21  {LT}
C_CC9          VC21 N13  {CC2}
R_RE8          VE22 0  {RE2}
I_It          VB22 0 DC 0Adc AC -1Aac
R_Rb9          VB11 VCC  {RB1}
C_Cc8          N21 VB12  {CC1}
L_LT2          VC12 VB22  {LT}
C_Cc10          N11 VB11  {CC1}
C_CE5          0 VE11  {CE1}
C_CTI3          N257744 VC12  {CTO}
Q_Q21          VC21 VB21 VE21 Q2N3904
C_CE4          0 VE12  {CE1}
C_CTI4          N12 VB21  {CTI}
R_RF4          N14 VB11  {RF}
C_CF3          N24 VE22  {CF}
R_RC8          VC12 VCC  {RC1}
R_Re7          VE12 0  {RE1}
R_RS4          N11 0  {Rs}
Q_Q11          VOC VB11 VE11 Q2N3904
R_RL3          N23 0  {RL}
R_RE10          VE21 0  {RE2}
R_RC9          VC21 VCC  {RC2}
V_VCC          VCC 0 DC={VCC}
R_RS3          N21 0  {Rs}
V_Vt1          N12 0 DC 0Vdc AC 1Vac
R_Rb10          0 VB11  {RB2}
C_CF4          N14 VE21  {CF}
R_RC10          VOC VCC  {RC1}
Q_Q12          VC12 VB12 VE12 Q2N3904
R_RL4          N13 0  {RL}
R_RC7          VC22 VCC  {RC2}
R_Re9          VE11 0  {RE1}
V_Vsc          N257744 0 DC 0Vdc AC 0Vac
.PARAM  re2=3.4k cto=1k rs=10k cap=1k rb2=15k re1=870 rb1=100k vcc=12 rl=1k
+  rc1=10k rc2=8k cti=1k cc1=1k cf=1k ce1=1k rf=10k cc2=1k lt=1e9
******* Main circuit ends here**************


************ Model for 2N3904 NPN BJT begins here*********************************
.model Q2N3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+               Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+               Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
************ Model for 2N3904 NPN BJT ends here***********************************

******** Analysis begins here****************
.AC  DEC   20  1 1G
.PROBE ; While plotting using the expression (1/(1/ V(VOC)+1/ I(V_Vsc))) for magnitude plot and
(-1/(1/ V(VOC)+1/ I(V_Vsc))) for phase plot
.END
******** Analysis ends here****************
```

The schematic of this example using method 2 is shown below.



Netlist:

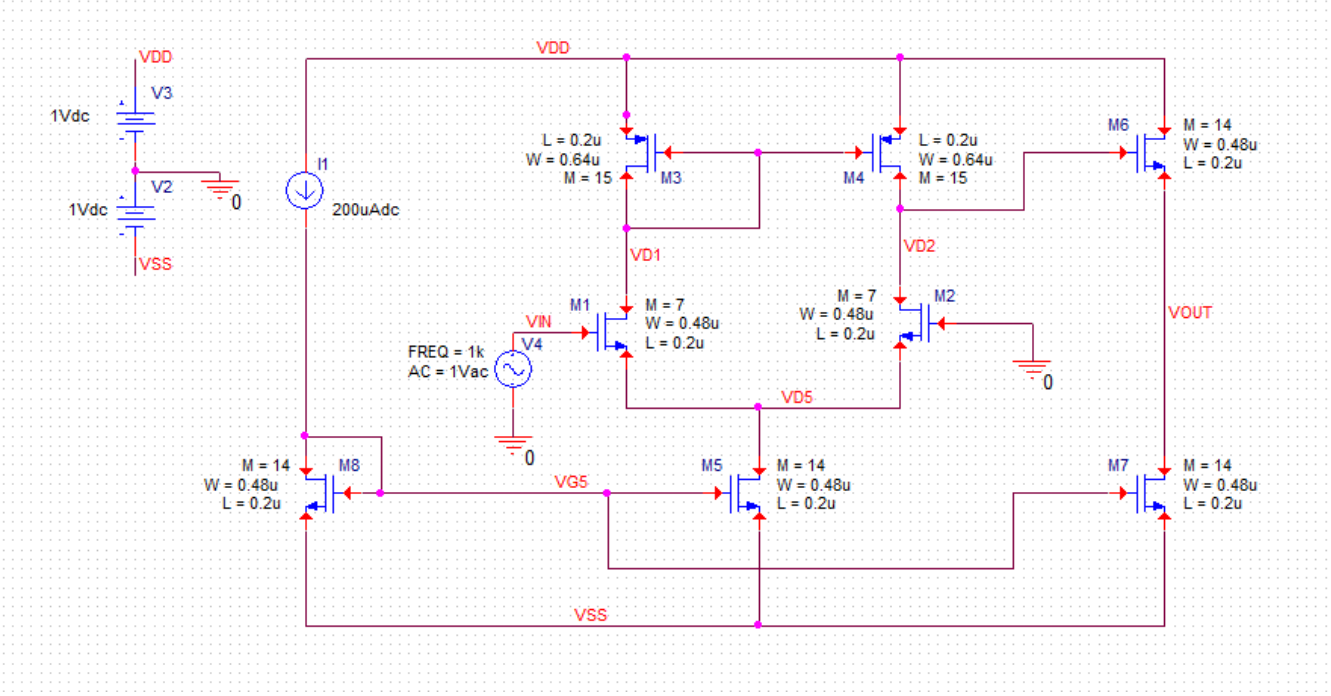
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
******Example S 11.1 Method 2 *************
******* Main circuit begins here**************
R_RL3          N23 0   {RL}
R_RF3          N24 VB12   {RF}
R_Rb9          VB11 VCC   {RB1}
L_LT2          VC12 VB22   {LT}
R_Rb7          VB12 VCC   {RB1}
R_RE10          VE21 0   {RE2}
```

```
R_RF4          N14 VB11  {RF}
R_RS4          N11 0  {Rs}
R_Re7          VE12 0  {RE1}
R_RC9          VC21 VCC  {RC2}
R_RE8          VE22 0  {RE2}
C_Cc8          N21 VB12  {CC1}
C_Cc10          N11 VB11  {CC1}
C_CC7          VC22 N23  {CC2}
R_RC7          VC22 VCC  {RC2}
Q_Q21          VC21 VB21 VE21 Q2N3904
Q_Q22          VC22 VB22 VE22 Q2N3904
C_CF3          N24 VE22  {CF}
C_CE4          0 VE12  {CE1}
R_Re9          VE11 0  {RE1}
R_RC8          VC12 VCC  {RC1}
Q_Q12          VC12 VB12 VE12 Q2N3904
R_RC10          VR VCC  {RC1}
C_CTI4          N12 VB21  {CTI}
R_Rb10          0 VB11  {RB2}
C_CC9          VC21 N13  {CC2}
C_CF4          N14 VE21  {CF}
V_VCC          VCC 0 DC={VCC}
V_Vt1          N12 0 DC 0Vdc AC 1Vac
R_RS3          N21 0  {Rs}
R_Rb8          0 VB12  {RB2}
R_RL4          N13 0  {RL}
C_CE5          0 VE11  {CE1}
Q_Q11          VR VB11 VE11 Q2N3904
L_LT3          VR VB21  {LT}
C_CTI3          VB22 VR  {CTO}
.PARAM  cto=1k re2=3.4k rs=10k cap=1k re1=870 rb2=15k rb1=100k vcc=12 rl=1k
+  rc1=10k rc2=8k cti=1k cc1=1k ce1=1k cf=1k rf=10k cc2=1k lt=1e9
******* Main circuit ends here**************

************ Model for 2N3904 NPN BJT begins here*********************************
.model Q2N3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+              Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+              Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+              Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
************ Model for 2N3904 NPN BJT ends here***********************************

******** Analysis begins here****************
.AC  DEC   20  1 1G
.PROBE
.END
******** Analysis ends here****************
```

Example S.11.2

The schematic of this example for finding Av is shown below.



Netlist:

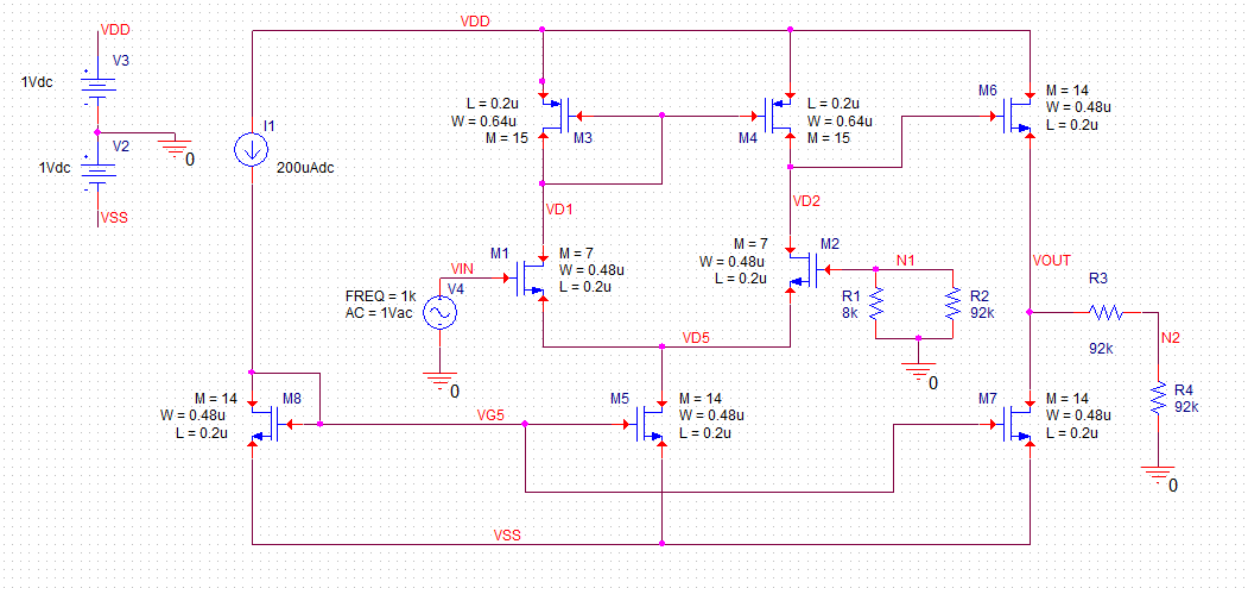
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 11.2 (Av) **********************
******* Main circuit begins here**************
V_V4          VIN 0  AC 1Vac
+SIN 0 1m 1k 0 0 0
M_M1          VD1 VIN VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=7
M_M3          VD1 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=15
I_I1          VDD VG5 DC 200uAdc
M_M5          VD5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
```

```
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
M_M8          VG5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
V_V2          0 VSS 1Vdc
M_M4          VD2 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=15
M_M7          VOUT VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
M_M2          VD2 0 VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=7
V_V3          VDD 0 1Vdc
M_M6          VDD VD2 VOUT 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
******* Main circuit ends here**************

*****************PMOS and NMOS models begin here*********************
.model NMOS4   NMOS(LEVEL= 1 VTO=0.5 GAMMA= 0.3  PHI=0.84
+ LAMBDA= 0.08
+ RS=    0.0
+ RD=    0.0
+ CBD=   0.0
+ CBS=   0.0
+ IS=    1.0e-14
+ PB=    0.9
+ CGSO=  0.3665e-9
+ CGDO=   0.3665e-9
+ CGBO=   0.38e-9
+ RSH=   0
+ CJ=    1.6e-3
+ MJ=    0.5
```

```
+ CJSW=  2.0405e-10
+ MJSW=  0.200379
+ JS=    8.38e-6
+ TOX= 4.08e-09
+ NSS=   0.0
+ TPG=   1.0
+ LD=    10e-9
+ U0 = 291
+ KF=    0.0
+ AF=    1.0
+ FC=    0.5
+ TNOM=  27
+ )

.model PMOS4   PMOS(LEVEL= 1 VTO=-0.5 KP=86.1e-6  GAMMA= 0.3
+ PHI=   0.8
+ LAMBDA= 0.11
+ RS=    0.0
+ RD=    0.0
+ CBD=   0.0
+ CBS=   0.0
+ IS=    1.0e-14
+ PB=    0.9
+ CGSO=  0.3426e-9
+ CGDO=  0.3426e-9
+ CGBO=  0.35e-9
+ RSH=   0
+ CJ=    1.01574e-03
+ MJ=    0.4490538
+ CJSW=  2.0405e-10
+ MJSW=  0.2931001
+ JS=    4e-7
+ NSS=   0.0
+ TPG=   1.0
+ LD=    10e-9
+ KF=    0.0
+ AF=    1.0
+ FC=    0.5
+ TNOM=  27
+ )
*****************PMOS and NMOS models end here*********************


******** Analysis begins here****************
.OP
.AC  DEC   20  1MEG 5G
.PROBE
.END
******** Analysis ends here****************
```

The schematic of this example for finding A is shown below.



Netlist:

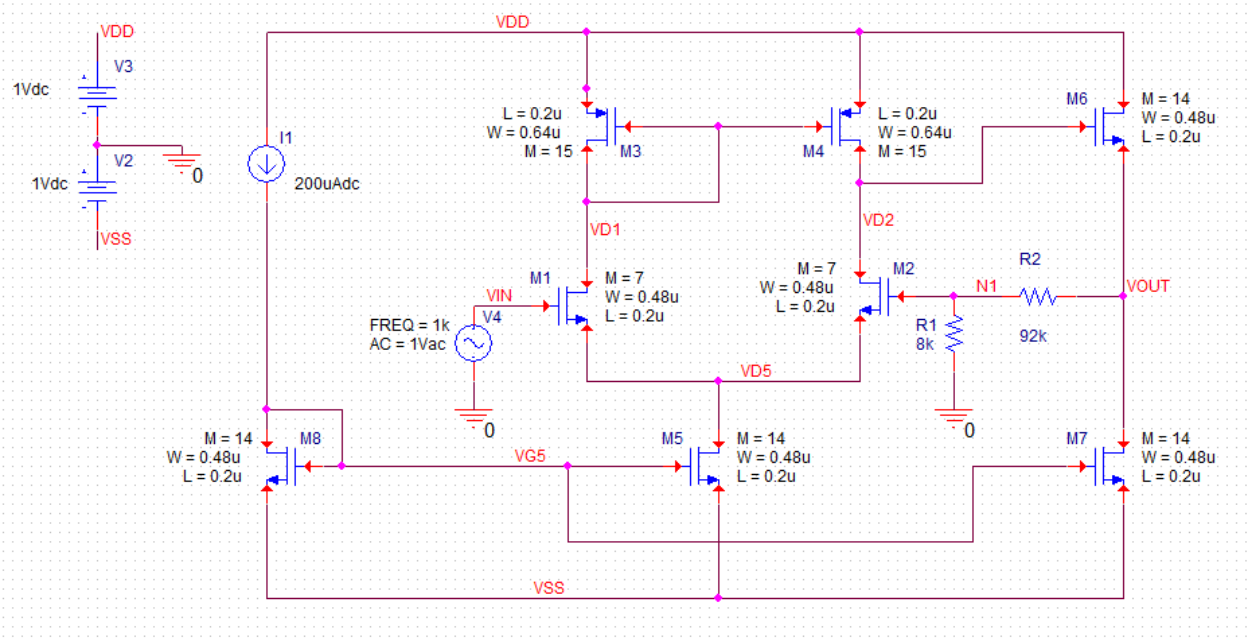
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 11.2 (A) **********************
******* Main circuit begins here**************
M_M6          VDD VD2 VOUT 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
M_M5          VD5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
I_I1          VDD VG5 DC 200uAdc
M_M3          VD1 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=15
V_V2          0 VSS 1Vdc
V_V4          VIN 0  AC 1Vac
+SIN 0 1m 1k 0 0 0
M_M1          VD1 VIN VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
```

```
+ PD=5.25E-6
+ PS=5.25E-6
+ M=7
V_V3         VDD 0 1Vdc
M_M8         VG5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
M_M2         VD2 N1 VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=7
M_M4         VD2 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=15
M_M7         VOUT VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
R_R1         0 N1  8k TC=0,0
R_R2         0 N1  92k TC=0,0
R_R3         N2 VOUT  92k TC=0,0
R_R4         0 N2  92k TC=0,0
******* Main circuit ends here**************
*****************PMOS and NMOS models begin here*********************
.model NMOS4   NMOS(LEVEL= 1 VTO=0.5 GAMMA= 0.3  PHI=0.84
+ LAMBDA= 0.08
+ RS=    0.0
+ RD=    0.0
+ CBD=   0.0
+ CBS=   0.0
+ IS=    1.0e-14
+ PB=    0.9
+ CGSO=  0.3665e-9
+ CGDO=   0.3665e-9
+ CGBO=   0.38e-9
+ RSH=   0
+ CJ=    1.6e-3
+ MJ=    0.5
+ CJSW=  2.0405e-10
+ MJSW=  0.200379
+ JS=    8.38e-6
+ TOX= 4.08e-09
+ NSS=   0.0
+ TPG=   1.0
+ LD=    10e-9
+ U0 = 291
```

```
+ KF=    0.0
+ AF=    1.0
+ FC=    0.5
+ TNOM=  27
+ )

.model PMOS4   PMOS(LEVEL= 1 VTO=-0.5 KP=86.1e-6  GAMMA= 0.3
+ PHI=   0.8
+ LAMBDA= 0.11
+ RS=    0.0
+ RD=    0.0
+ CBD=   0.0
+ CBS=   0.0
+ IS=    1.0e-14
+ PB=    0.9
+ CGSO=  0.3426e-9
+ CGDO=  0.3426e-9
+ CGBO=  0.35e-9
+ RSH=   0
+ CJ=    1.01574e-03
+ MJ=    0.4490538
+ CJSW=  2.0405e-10
+ MJSW=  0.2931001
+ JS=    4e-7
+ NSS=   0.0
+ TPG=   1.0
+ LD=    10e-9
+ KF=    0.0
+ AF=    1.0
+ FC=    0.5
+ TNOM=  27
+ )
*****************PMOS and NMOS models end here*********************
******** Analysis begins here****************
.OP
.AC  DEC   20  1MEG 5G
.PROBE
.END
******** Analysis ends here****************
```

The schematic for finding Af in this example is shown below.



Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

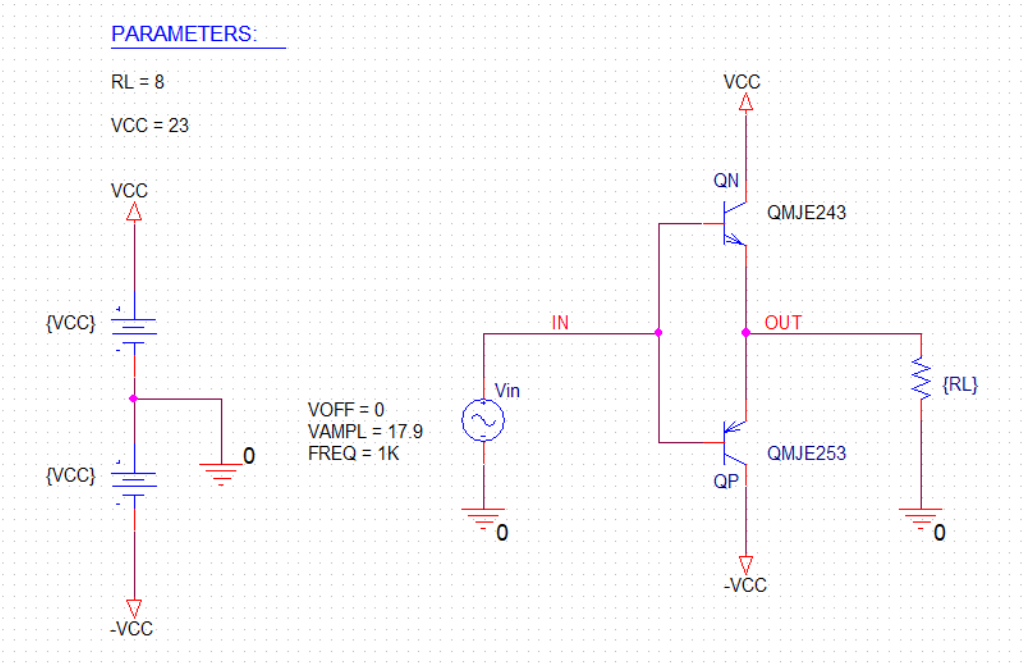
```
********Example S 11.2 (Af) **********************
******* Main circuit begins here**************
R_R1          0 N1   8k TC=0,0
R_R2          VOUT N1   92k TC=0,0
M_M4          VD2 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=15
M_M7          VOUT VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
V_V3          VDD 0 1Vdc
V_V4          VIN 0  AC 1Vac
+SIN 0 1m 1k 0 0 0
M_M6          VDD VD2 VOUT 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
```

```
+ M=14
V_V2          0 VSS 1Vdc
M_M1          VD1 VIN VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=7
M_M8          VG5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
M_M2          VD2 N1 VD5 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=7
I_I1          VDD VG5 DC 200uAdc
M_M3          VD1 VD1 VDD VDD PMOS4
+ L=0.2u
+ W=0.64u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M=15
M_M5          VD5 VG5 VSS 0 NMOS4
+ L=0.2u
+ W=0.48u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M=14
******* Main circuit ends here**************

*****************PMOS and NMOS models begin here*********************
.model NMOS4   NMOS(LEVEL= 1 VTO=0.5 GAMMA= 0.3  PHI=0.84
+ LAMBDA= 0.08
+ RS=    0.0
+ RD=    0.0
+ CBD=   0.0
+ CBS=   0.0
+ IS=    1.0e-14
+ PB=    0.9
+ CGSO=  0.3665e-9
+ CGDO=   0.3665e-9
+ CGBO=   0.38e-9
+ RSH=   0
+ CJ=    1.6e-3
+ MJ=    0.5
+ CJSW=  2.0405e-10
+ MJSW=  0.200379
+ JS=    8.38e-6
+ TOX= 4.08e-09
```

```
+ NSS=   0.0
+ TPG=   1.0
+ LD=    10e-9
+ U0 = 291
+ KF=    0.0
+ AF=    1.0
+ FC=    0.5
+ TNOM=  27
+ )

.model PMOS4   PMOS(LEVEL= 1 VTO=-0.5 KP=86.1e-6  GAMMA= 0.3
+ PHI=   0.8
+ LAMBDA= 0.11
+ RS=    0.0
+ RD=    0.0
+ CBD=   0.0
+ CBS=   0.0
+ IS=    1.0e-14
+ PB=    0.9
+ CGSO=  0.3426e-9
+ CGDO=  0.3426e-9
+ CGBO=  0.35e-9
+ RSH=   0
+ CJ=    1.01574e-03
+ MJ=    0.4490538
+ CJSW=  2.0405e-10
+ MJSW=  0.2931001
+ JS=    4e-7
+ NSS=   0.0
+ TPG=   1.0
+ LD=    10e-9
+ KF=    0.0
+ AF=    1.0
+ FC=    0.5
+ TNOM=  27
+ )
*****************PMOS and NMOS models end here*********************

******** Analysis begins here****************
.OP
.AC  DEC   20  1MEG 5G
.PROBE
.END
******** Analysis ends here****************
```

Example S.12.1

The schematic of this example is shown below.



Netlist:

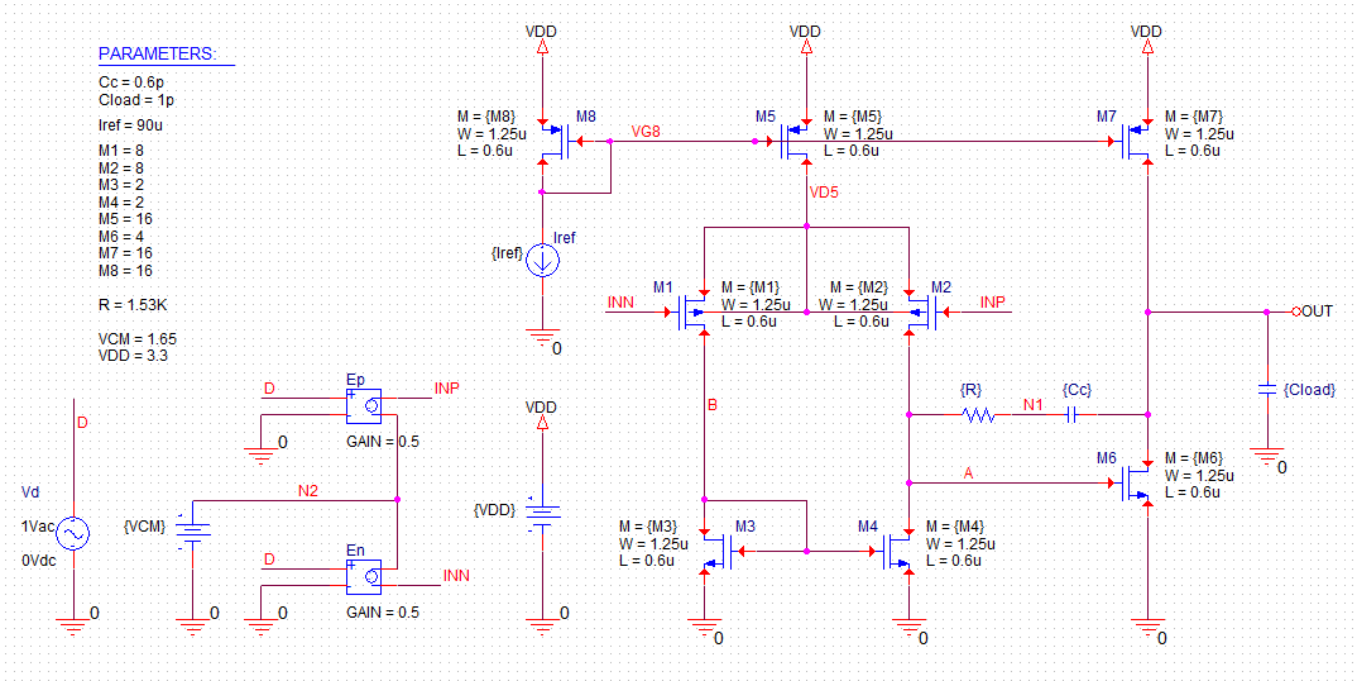
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 12.1 ***************
******* Main circuit begins here**************
Q_QN          VCC IN OUT QMJE243
V_-VCC          0 -VCC {VCC}
R_RL          OUT 0  {RL}
V_VCC          VCC 0 {VCC}
Q_QP          -VCC IN OUT QMJE253
V_Vin          IN 0
+SIN 0 17.9 1K 0 0 0
.PARAM  vcc=23 rl=8
******* Main circuit ends here**************

********Model for MJE243 Power NPN BJT (from ON Semiconductor) begins here*****
.model  QMJE243 NPN(
+       IS=1.27357e-12 BF=188.792 NF=1.05658 VAF=13.5417
+       IKF=0.442678 ISE=1e-16 NE=4 BR=1.73115
+       NR=1.04113 VAR=135.417 IKR=1.00889 ISC=1e-16
+       NC=2.93725 RB=193.999 IRB=5.29235e-05 RBM=0.000841015
+       RE=9.44257e-05 RC=0.216999 XTB=1.16682 XTI=0.80411
+       EG=1.05 CJE=2.19516e-10 VJE=0.99 MJE=0.39332
+       TF=1.51916e-09 XTF=1.21445 VTF=11.3491 ITF=0.0098534
+       CJC=7.43909e-11 VJC=0.4 MJC=0.287382 XCJC=0.799998
+       FC=0.577401 CJS=0 VJS=0.75 MJS=0.5
+       TR=7.76174e-07 PTF=0 KF=0 AF=1)
********Model for MJE243 Power NPN BJT (from ON Semiconductor) ends here*****
```

```
******** Model for MJE253 Power PNP BJT (from ON Semiconductor) begins here*****
.model  QMJE253 PNP(
+       IS=2.52937e-13 BF=54.36 NF=1.01478 VAF=4.91894
+       IKF=0.84154 ISE=6.32316e-13 NE=3.6001 BR=3.71504
+       NR=1.15303 VAR=49.1894 IKR=4.42705 ISC=6.32316e-13
+       NC=2.93783 RB=417.673 IRB=7.10249e-06 RBM=0.000992345
+       RE=6.68257e-05 RC=0.262081 XTB=1.32735 XTI=0.01
+       EG=1.05 CJE=1.57797e-10 VJE=0.99 MJE=0.339209
+       TF=2.58603e-09 XTF=1.5 VTF=0.999999 ITF=1
+       CJC=6.54856e-11 VJC=0.0328604 MJC=0.208693 XCJC=0.8
+       FC=0.532891 CJS=0 VJS=0.75 MJS=0.5
+       TR=7.83777e-07 PTF=0 KF=0 AF=1)
******** Model for MJE253 Power PNP BJT (from ON Semiconductor) ends here*****

******** Analysis begins here****************
.TRAN   0.01mS  3mS
*.DC [LIN] V_Vin  -10 10 1m
.PROBE
.END
******** Analysis ends here****************
```

Example S.13.1

The schematic of this example for AC analysis is shown below.



Netlist:

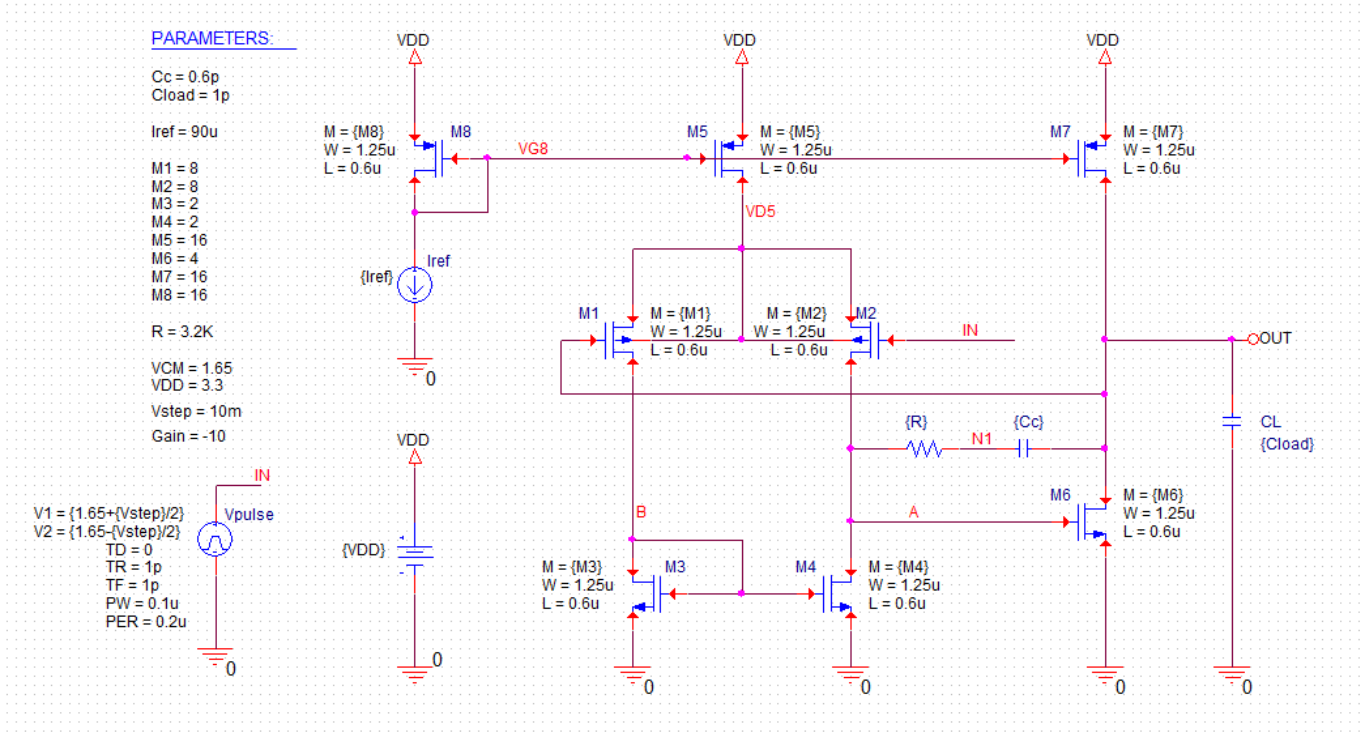
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 13.1 AC ***************
******* Main circuit begins here**************
V_VCM          N2 0 {VCM}
V_VCC          VDD 0 {VDD}
M_M8          VG8 VG8 VDD VDD PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M8}
C_CL          0 OUT  {Cload}
M_M7          OUT VG8 VDD VDD PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M7}
E_En          N2 INN D 0 0.5
V_Vd          D 0 DC 0Vdc AC 1Vac
I_Iref          VG8 0 DC {Iref}
M_M5          VD5 VG8 VDD VDD PMOS0P5
```

```
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M5}
C_Cc          N1 OUT  {Cc}
M_M2          A INP VD5 VD5 PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M2}
M_M4          A B 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M4}
M_M1          B INN VD5 VD5 PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M1}
M_M3          B B 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M3}
M_M6          OUT A 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M6}
E_Ep          INP N2 D 0 0.5
R_R          A N1  {R}
.PARAM  m8=16 vcm=1.65 iref=90u cc=0.6p m6=4 m7=16 m4=2 vdd=3.3 m5=16 m2=8
+  cload=1p m3=2 m1=8 r=1.53k
******* Main circuit ends here**************

************Model for NMOS in 0.5um CMOS Technology begins here*****************
*               (created by Anas Hamoui & Olivier Trescases)
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+               LD=0.08E-06 WD=0 UO=460 LAMBDA=0.1 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+               CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+               CGSO=0.4E-9)
************Model for NMOS in 0.5um CMOS Technology ends here*****************

************Model for PMOS in 0.5um CMOS Technology begins here*****************
*               (created by Anas Hamoui & Olivier Trescases)
```

```
.model PMOS0P5 PMOS(Level=1 VTO=-0.8 GAMMA=0.45 PHI=0.8
+               LD=0.09E-06 WD=0 UO=115 LAMBDA=0.2 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+               CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+               CGSO=0.35E-9)
************Model for PMOS in 0.5um CMOS Technology ends here*****************

******** Analysis begins here***************
.OP
.AC  DEC   20  1 1G
.PROBE
.END
******** Analysis ends here***************
```

The schematic of this example for transient analysis is shown below.



Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

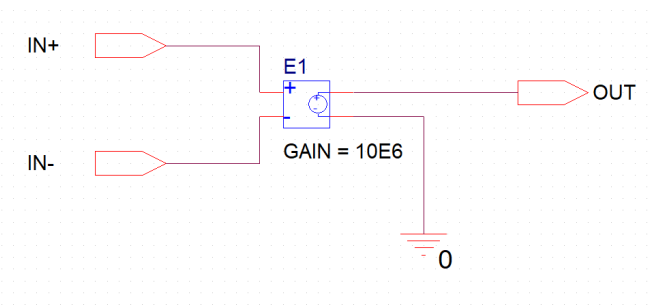
```
********Example PS 13.1 TRANS ***************
******* Main circuit begins here**************
C_CL          0 OUT  {Cload}
R_R          A N1  {R}
V_VCC          VDD 0 {VDD}
M_M8          VG8 VG8 VDD VDD PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
```

```
+ PS=5.25E-6
+ M={M8}
V_Vpulse         IN 0 DC 1.65
+PULSE {1.65+{Vstep}/2} {1.65-{Vstep}/2} 0 1p 1p 0.1u 0.2u
M_M6         OUT A 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M6}
I_Iref          VG8 0 DC {Iref}
M_M2         A IN VD5 VD5 PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M2}
M_M5         VD5 VG8 VDD VDD PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M5}
M_M1         B OUT VD5 VD5 PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M1}
M_M4         A B 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M4}
C_Cc         N1 OUT  {Cc}
M_M3         B B 0 0 NMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={M3}
M_M7         OUT VG8 VDD VDD PMOS0P5
+ L=0.6u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={M7}
.PARAM  m8=16 vcm=1.65 iref=90u cc=0.6p vstep=10m m6=4 m7=16 m4=2 vdd=3.3 m5=16
+  m2=8 cload=1p m3=2 m1=8 gain=-10 r=3.2k
```

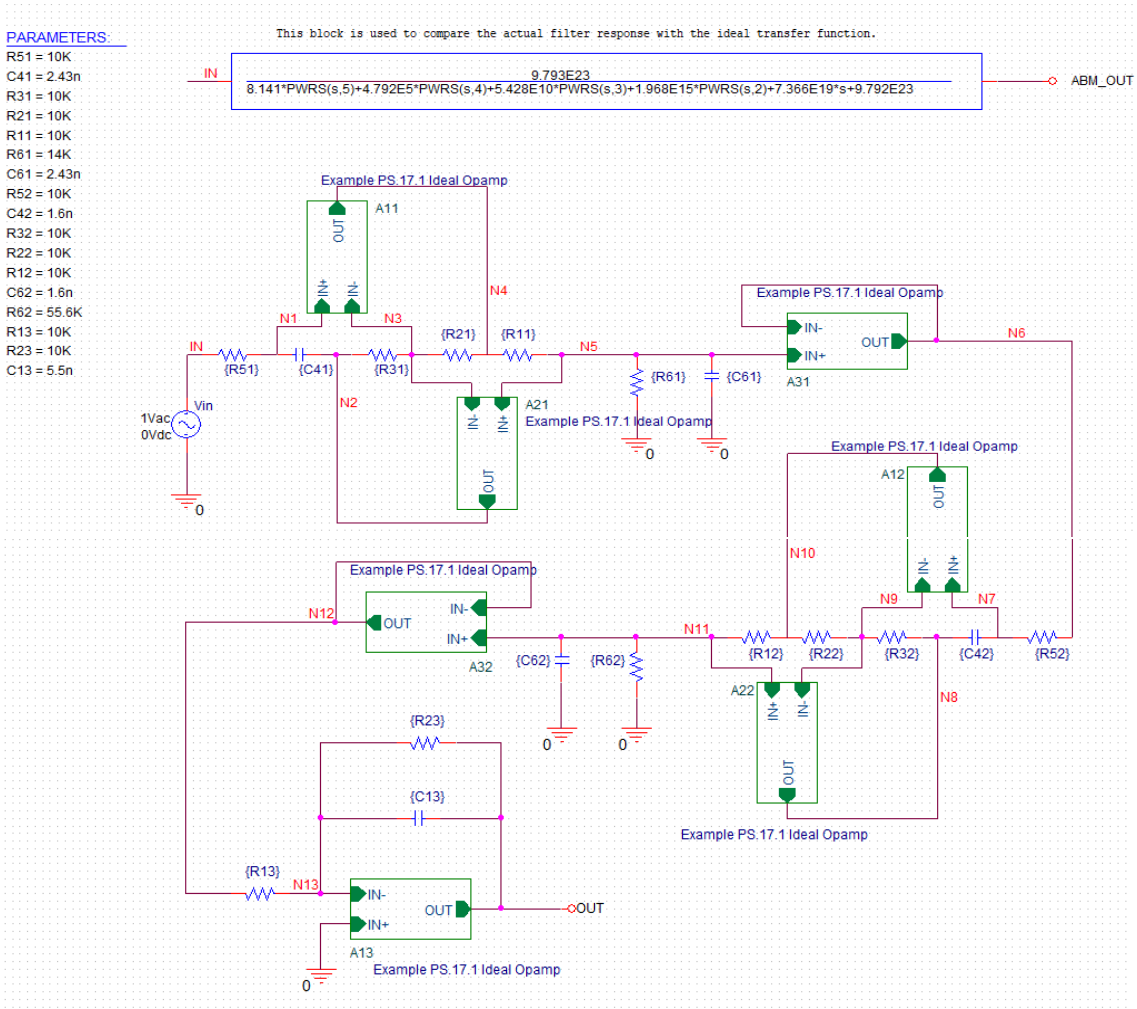
```
******* Main circuit ends here**************

************Model for NMOS in 0.5um CMOS Technology begins here*****************
*              (created by Anas Hamoui & Olivier Trescases)
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+              LD=0.08E-06 WD=0 UO=460 LAMBDA=0.1 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+              CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+              CGSO=0.4E-9)
************Model for NMOS in 0.5um CMOS Technology ends here*****************

************Model for PMOS in 0.5um CMOS Technology begins here*****************
*              (created by Anas Hamoui & Olivier Trescases)
.model PMOS0P5 PMOS(Level=1 VTO=-0.8 GAMMA=0.45 PHI=0.8
+              LD=0.09E-06 WD=0 UO=115 LAMBDA=0.2 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+              CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+              CGSO=0.35E-9)
************Model for PMOS in 0.5um CMOS Technology ends here*****************

******** Analysis begins here****************
.TRAN   0.01nS  400nS
.PROBE
.END
******** Analysis ends here****************
```

Example S.14.1

The schematic of the op amp macro model for this example is shown below.



The schematic of the main circuit for this example is shown below.



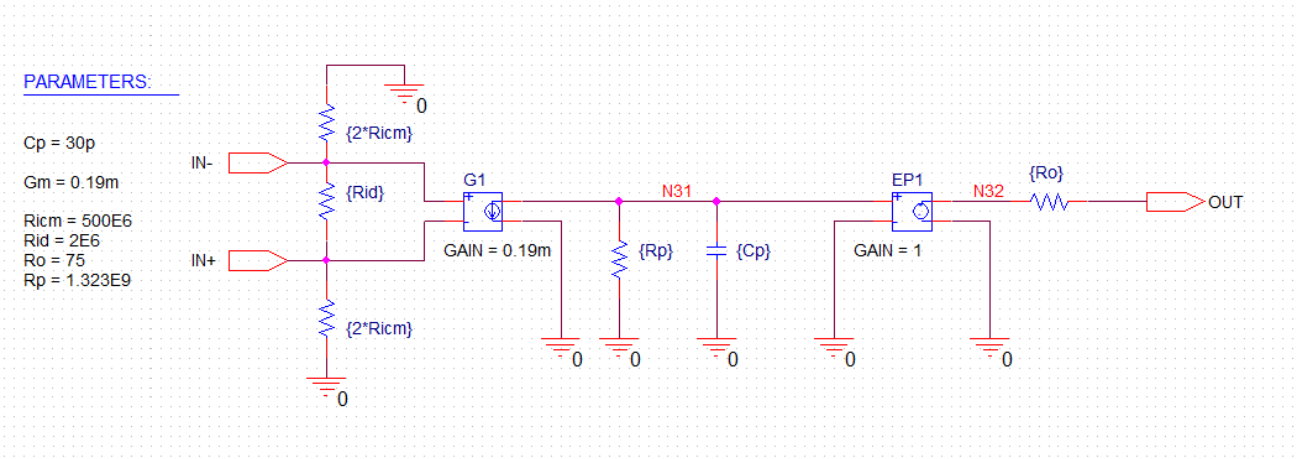
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

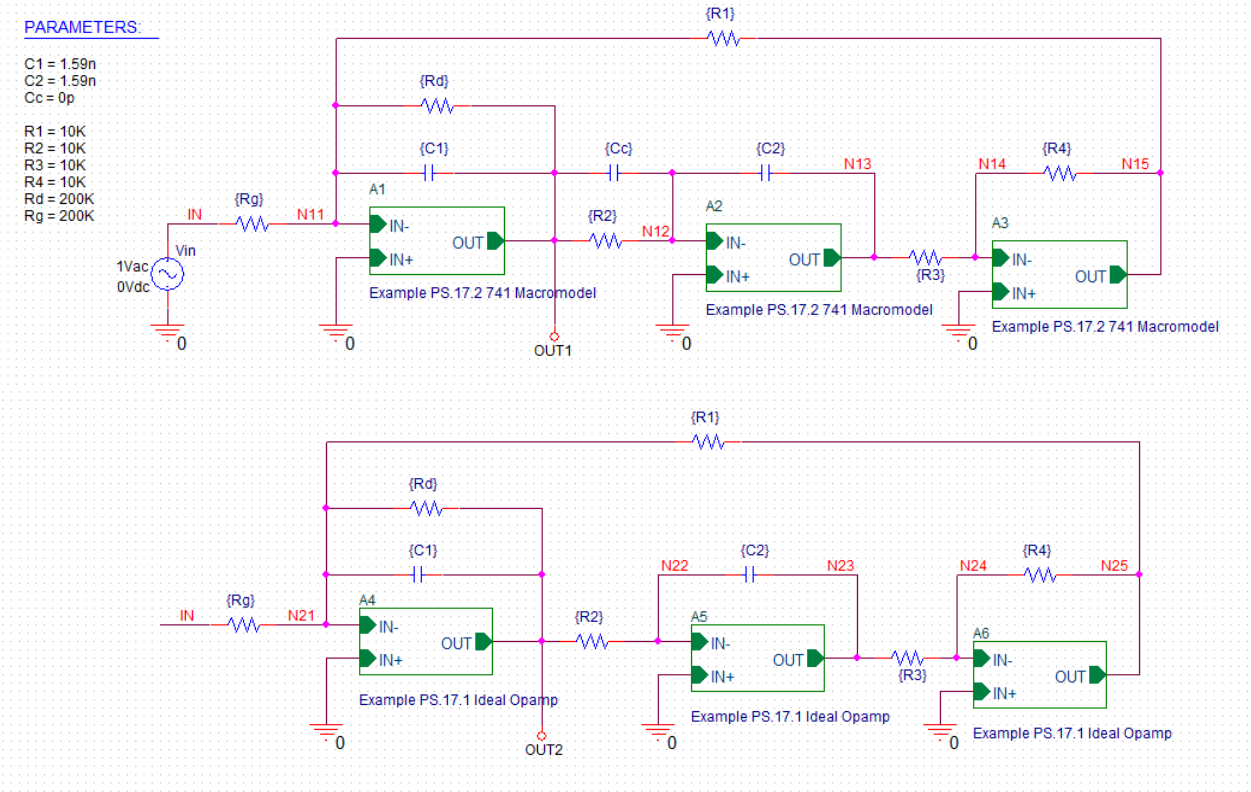
```
********Example S 14.1 ***************
******* Main circuit begins here**************
R_R8          N8 N9  {R32}
C_C5          OUT N13  {C13}
R_R3          N3 N4  {R21}
V_Vin          IN 0 DC 0Vdc AC 1Vac
R_R11          OUT N13  {R23}
R_R5          0 N5  {R61}
R_R7          N9 N10  {R22}
R_R4          N4 N5  {R11}
R_R6          N10 N11  {R12}
C_C1          N1 N2  {C41}
C_C3          N7 N8  {C42}
E_LAPLACE1          ABM_OUT 0 LAPLACE {V(IN)}
+
{(9.793E23)/(8.141*PWRS(s,5)+4.792E5*PWRS(s,4)+5.428E10*PWRS(s,3)+1.968E15*PWRS(s,2)+7.366E19*s+9
.792E23)}
R_R1          IN N1  {R51}
C_C4          0 N11  {C62}
R_R9          N6 N7  {R52}
R_R2          N2 N3  {R31}
R_R10          0 N11  {R62}
R_R12          N13 N12  {R13}
C_C2          0 N5  {C61}
X_A11            N3 N1 N4 OPAMP_MACRO
X_A31            N6 N5 N6 OPAMP_MACRO
X_A21            N3 N5 N2 OPAMP_MACRO
X_A12            N9 N7 N10 OPAMP_MACRO
X_A32            N12 N11 N12 OPAMP_MACRO
X_A22            N9 N11 N8 OPAMP_MACRO
X_A13            N13 0 OUT OPAMP_MACRO

.PARAM  c41=2.43n c42=1.6n r62=55.6k r23=10k r61=14k r22=10k r21=10k r31=10k
+  r52=10k r32=10k c62=1.6n r51=10k r12=10k c13=5.5n c61=2.43n r13=10k r11=10k
******* Main circuit ends here **************

******* Opamp macro model begins here **************
.SUBCKT OPAMP_MACRO    IN- IN+ OUT
E_E1          OUT 0 IN+ IN- 10E6
.ENDS
******* Opamp macro model ends here **************

******** Analysis begins here****************
.AC  DEC   100  0.1 20K
.PROBE
.END
******** Analysis ends here****************
```

Example S.14.2

The schematic of the 741 op amp macro model for this example is shown below.



The schematic of the main circuit for this example is shown below.



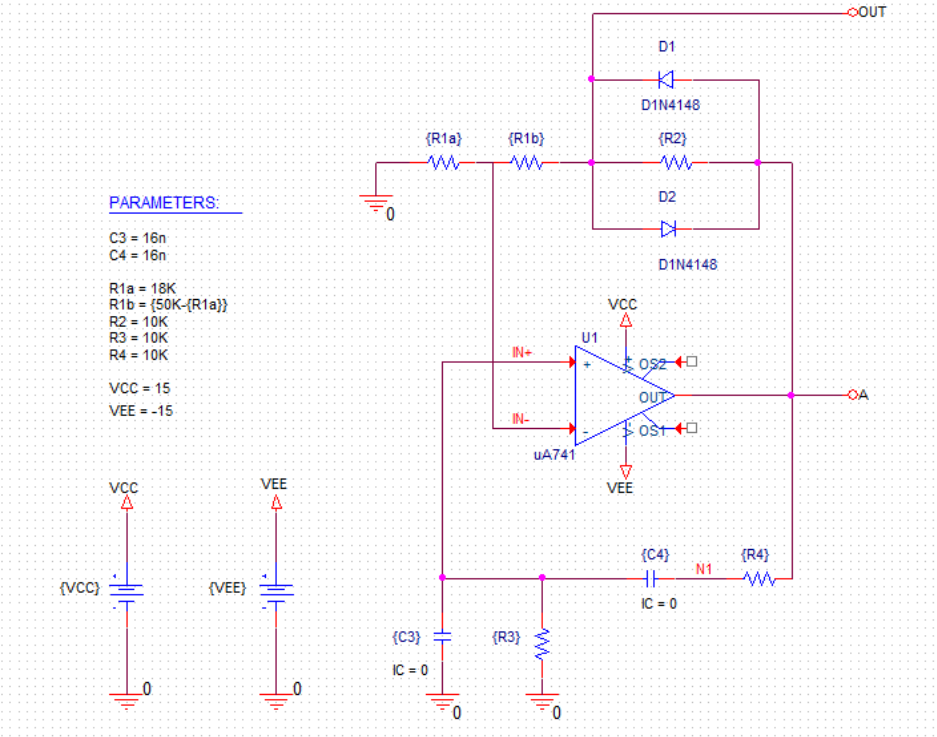
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 14.2 ***************
******* Main circuit begins here**************
R_R4          N14 N15  {R4}
R_R8          OUT2 N22  {R2}
V_Vin          IN 0 DC 0Vdc AC 1Vac
R_R3          N13 N14  {R3}
C_C5          OUT1 N12  {Cc}
R_R12          IN N21  {Rg}
C_C3          N21 OUT2  {C1}
C_C2          N12 N13  {C2}
R_R9          N23 N24  {R3}
R_R6          IN N11  {Rg}
R_R2          OUT1 N12  {R2}
R_R5          N11 N15  {R1}
R_R7          N21 OUT2  {Rd}
R_R1          N11 OUT1  {Rd}
C_C1          N11 OUT1  {C1}
R_R11          N21 N25  {R1}
R_R10          N24 N25  {R4}
C_C4          N22 N23  {C2}
X_A1            0 N11 OUT1     741_OPAMP_MACRO
X_A2            0 N12   N13 741_OPAMP_MACRO
X_A3            0 N14   N15     741_OPAMP_MACRO
X_A4            0 N21 OUT2     IDEAL_OPAMP_MACRO
X_A5            0 N22   N23 IDEAL_OPAMP_MACRO
X_A6            0 N24   N25     IDEAL_OPAMP_MACRO
.PARAM  cc=0p c1=1.59n r4=10k c2=1.59n r3=10k r2=10k r1=10k rg=200k rd=200k
******* Main circuit ends here **************

*******741 Opamp macro model begins here **************
.SUBCKT 741_OPAMP_MACRO    IN+ IN- OUT
R_R4          IN- 0  {2*Ricm}
R_R5          0 IN+  {2*Ricm}
G_G1          N31 0 IN- IN+ 0.19m
R_R1          N32 OUT  {Ro}
R_R2          0 N31  {Rp}
R_R3          IN+ IN-  {Rid}
C_C2          0 N31  {Cp}
E_EP1          N32 0 N31 0 1
.PARAM  ricm=500e6 gm=0.19m ro=75 rp=1.323e9 rid=2e6 cp=30p
.ENDS
*******741 Opamp macro model ends here **************

******* Ideal Opamp macro model begins here **************
.SUBCKT IDEAL_OPAMP_MACRO    IN+ IN- OUT
E_E1          OUT 0 IN+ IN- 10E6
.ENDS
******* Ideal Opamp macro model ends here **************

******** Analysis begins here***************
.AC  DEC   1000  0.1 20K
.PROBE
.END
******** Analysis ends here***************
```

Example S.15.1

The schematic of this example is shown below.



Netlist:

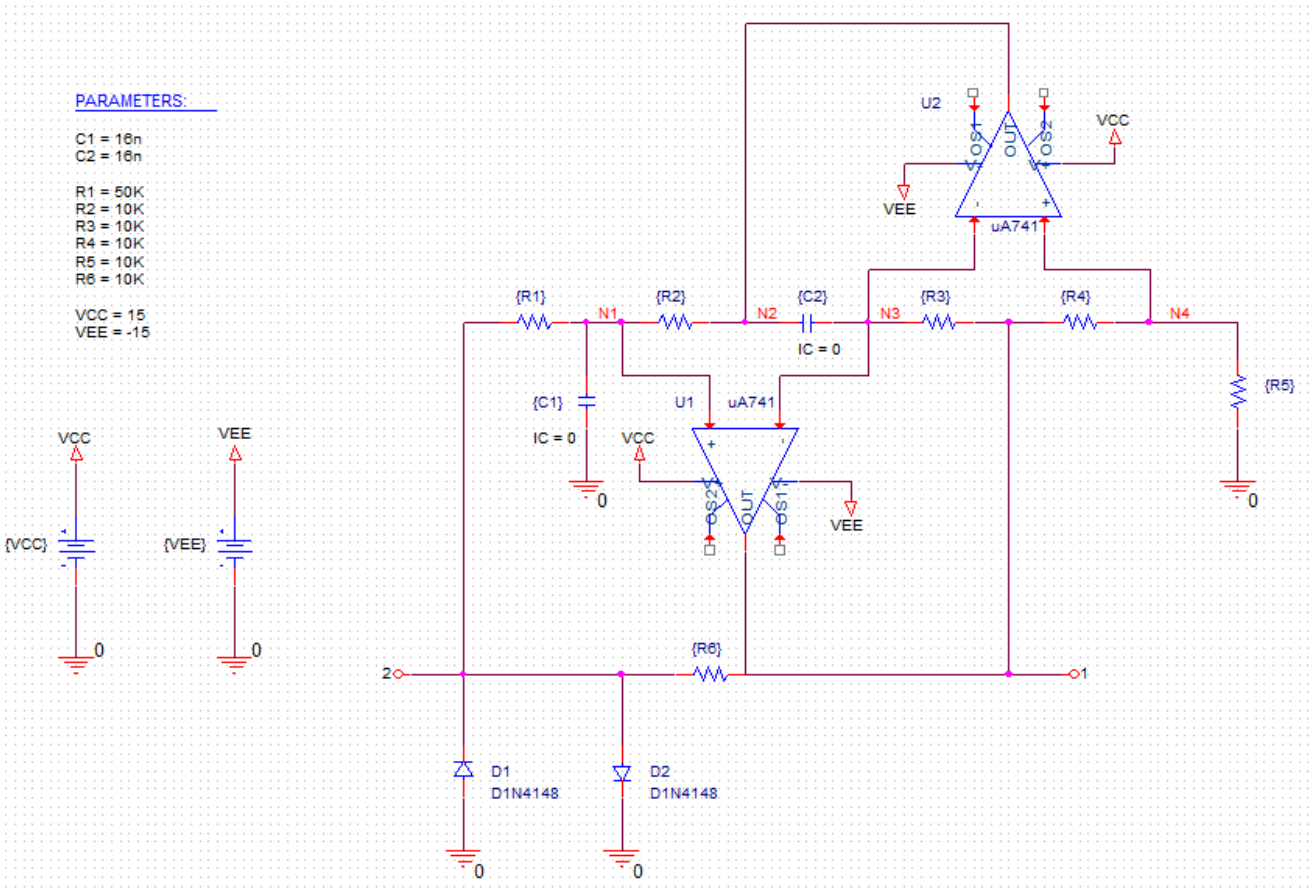
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 15.1 ***************
******* Main circuit begins here**************
X_U1          IN+ IN- VCC VEE A uA741
R_R1a          0 IN-  {R1a}
V_VCC          VCC 0 {VCC}
R_R1b          IN- OUT  {R1b}
R_R2          OUT A  {R2}
R_R4          N1 A  {R4}
D_D2          OUT A D1N4148
R_R3          0 IN+  {R3}
C_C4          N1 IN+  {C4} IC=0
C_C3          0 IN+  {C3} IC=0
D_D1          A OUT D1N4148
V_VEE          VEE 0 {VEE}
.PARAM  r1a=18k vee=-15 r4=10k r3=10k c3=16n r2=10k vcc=15 r1b={50k-{r1a}}
+  c4=16n
******* Main circuit ends here **************

******** Model of uA741 begins here****************
* connections:   non-inverting input
```

```
*                |  inverting input
*                |  |  positive power supply
*                |  |  |  negative power supply
*                |  |  |  |  output
*                |  |  |  |  |
.subckt uA741    1 2 3 4 5
*
c1   11 12 8.661E-12
c2    6  7 30.00E-12
dc    5 53 dx
de   54  5 dx
dlp  90 91 dx
dln  92 90 dx
dp    4  3 dx
egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
fb    7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -10E6 10E6 10E6 -10E6
ga    6  0 11 12 188.5E-6
gcm   0  6 10 99 5.961E-9
iee  10  4 dc 15.16E-6
hlim 90  0 vlim 1K
q1   11  2 13 qx
q2   12  1 14 qx
r2    6  9 100.0E3
rc1   3 11 5.305E3
rc2   3 12 5.305E3
re1  13 10 1.836E3
re2  14 10 1.836E3
ree  10 99 13.19E6
ro1   8  5 50
ro2   7 99 100
rp    3  4 18.16E3
vb    9  0 dc 0
vc    3 53 dc 1
ve   54  4 dc 1
vlim  7  8 dc 0
vlp  91  0 dc 40
vln   0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=93.75)
.ends
******** Model of uA741 ends here****************

******** Model of 1N4148 Diode (from EVAL library in PSpice) begins here****************
.model D1N4148  D(Is=2.682n N=1.836 Rs=.5664 Ikf=44.17m Xti=3 Eg=1.11 Cjo=4p
+               M=.3333 Vj=.5 Fc=.5 Isr=1.565n Nr=2 Bv=100 Ibv=100u Tt=11.54n)
******** Model of 1N4148 Diode (from EVAL library in PSpice) ends here****************

******** Analysis begins here****************
.TRAN 0.001mS  20mS
.PROBE
.END
******** Analysis ends here****************
```

Example S.15.2

The schematic of this example is shown below.



Netlist:

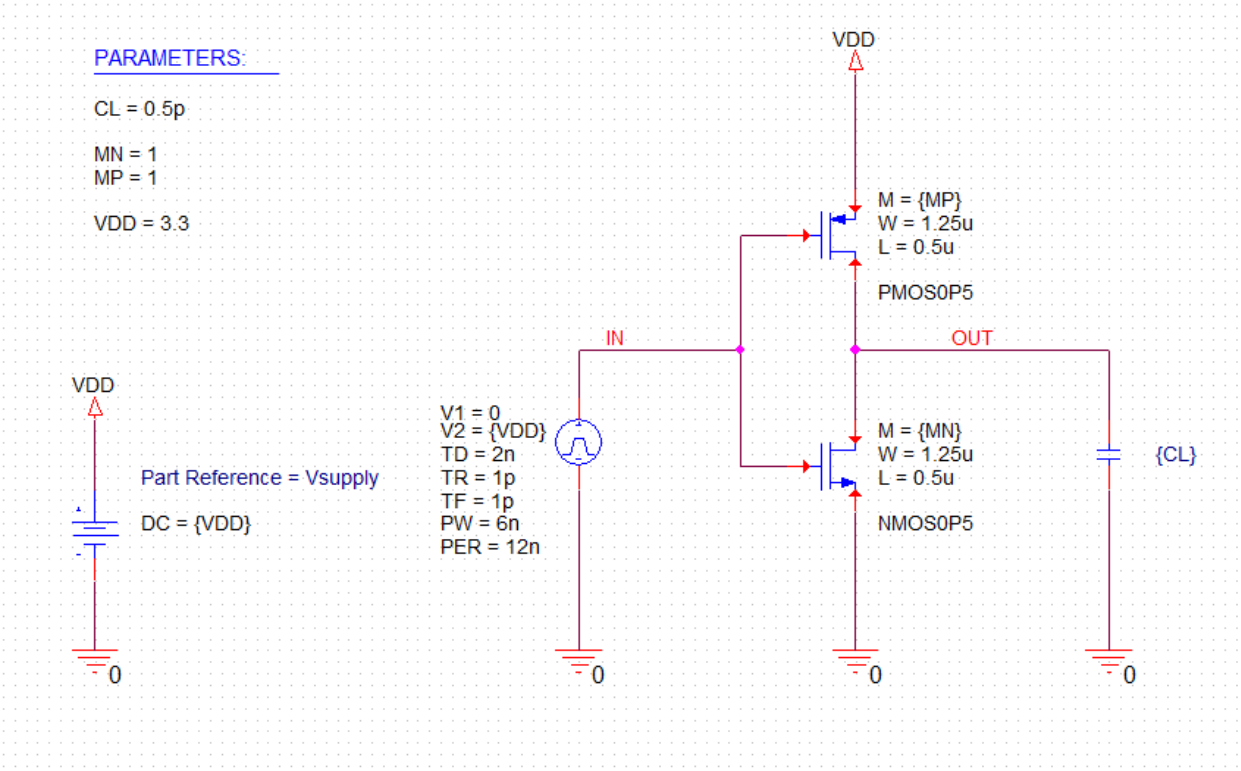
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 15.2 ***************
******* Main circuit begins here**************
X_U1          N1 N3 VCC VEE 1 uA741
C_C4          N3 N2  {C2} IC=0
R_R1a5          N3 1  {R3}
R_R1a6          1 N4  {R4}
V_VEE          VEE 0 {VEE}
X_U2          N4 N3 VCC VEE N2 uA741
C_C3          0 N1  {C1} IC=0
V_VCC          VCC 0 {VCC}
R_R1a4          2 1  {R6}
R_R1a7          0 N4  {R5}
D_D2          2 0 D1N4148
R_R1a          N1 N2  {R2}
```

```
R_R1         2 N1  {R1}
D_D1         0 2 D1N4148
.PARAM  vee=-15 r6=10k r5=10k c1=16n r4=10k r3=10k c2=16n vcc=15 r2=10k r1=50k
******* Main circuit ends here **************

******** Model of uA741 begins here****************
* connections:   non-inverting input
*                |  inverting input
*                |  |  positive power supply
*                |  |  |  negative power supply
*                |  |  |  |  output
*                |  |  |  |  |
.subckt uA741    1 2 3 4 5
*
c1   11 12 8.661E-12
c2    6  7 30.00E-12
dc    5 53 dx
de   54  5 dx
dlp  90 91 dx
dln  92 90 dx
dp    4  3 dx
egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
fb    7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -10E6 10E6 10E6 -10E6
ga    6  0 11 12 188.5E-6
gcm   0  6 10 99 5.961E-9
iee  10  4 dc 15.16E-6
hlim 90  0 vlim 1K
q1   11  2 13 qx
q2   12  1 14 qx
r2    6  9 100.0E3
rc1   3 11 5.305E3
rc2   3 12 5.305E3
re1  13 10 1.836E3
re2  14 10 1.836E3
ree  10 99 13.19E6
ro1   8  5 50
ro2   7 99 100
rp    3  4 18.16E3
vb    9  0 dc 0
vc    3 53 dc 1
ve   54  4 dc 1
vlim  7  8 dc 0
vlp  91  0 dc 40
vln   0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=93.75)
.ends
******** Model of uA741 ends here****************

******** Model of 1N4148 Diode (from EVAL library in PSpice) begins here****************
.model D1N4148  D(Is=2.682n N=1.836 Rs=.5664 Ikf=44.17m Xti=3 Eg=1.11 Cjo=4p
+               M=.3333 Vj=.5 Fc=.5 Isr=1.565n Nr=2 Bv=100 Ibv=100u Tt=11.54n)
******** Model of 1N4148 Diode (from EVAL library in PSpice) ends here****************

******** Analysis begins here****************
.TRAN 0.001mS  50mS
.PROBE
.END
******** Analysis ends here****************
```

Example S.16.1

The schematic of this example is shown below.



Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Example S 16.1 ***************
******* Main circuit begins here**************
V_Vin          IN 0
+PULSE 0 {VDD} 2n 1p 1p 6n 12n
M_M1          OUT IN VDD VDD PMOS0P5
+ L=0.5u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25e-6
+ PS=5.25E-6
+ M={MP}
C_C10          0 OUT  {CL}
M_M2          OUT IN 0 0 NMOS0P5
+ L=0.5u
+ W=1.25u
+ AD=1.72E-12
+ AS=1.72E-12
+ PD=5.25E-6
+ PS=5.25E-6
+ M={MN}
```

```
V_Vsupply         VDD 0 {VDD}
.PARAM  cl=0.5p vdd=3.3 mp=1 mn=1
******* Main circuit ends here**************

************Model for NMOS in 0.5um CMOS Technology begins here*****************
*              (created by Anas Hamoui & Olivier Trescases)
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+              LD=0.08E-06 WD=0 UO=460 LAMBDA=0.1 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+              CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+              CGSO=0.4E-9)
************Model for NMOS in 0.5um CMOS Technology ends here*****************

************Model for PMOS in 0.5um CMOS Technology begins here*****************
*              (created by Anas Hamoui & Olivier Trescases)
.model PMOS0P5 PMOS(Level=1 VTO=-0.8 GAMMA=0.45 PHI=0.8
+              LD=0.09E-06 WD=0 UO=115 LAMBDA=0.2 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+              CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+              CGSO=0.35E-9)
************Model for PMOS in 0.5um CMOS Technology ends here*****************

******** Analysis begins here****************
.DC [LIN] V_Vin  0 3.3 10m
*.TRAN  0.01nS  14nS
.PROBE
.END
******** Analysis ends here****************
```